



SSC8132GN1

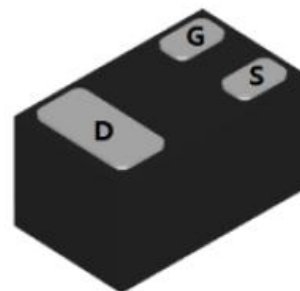
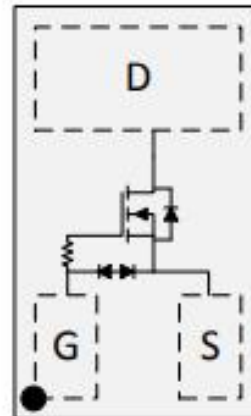
N-Channel Enhancement Mode MOSFET with ESD protection

➤ Features

VDS	VGS	RDS(on) Typ.	ID	ESD
35V	±10V	320mR@10V	2A	1K
		350mR@4V5		
		430mR@2V5		

➤ Pin configuration

Top view



Bottom View

➤ Description

This device is a N-Channel enhancement mode MOSFET which is produced with high cell density and DMOS trench technology. This device particularly suits low voltage applications, especially for battery powered circuits, the tiny and thin outline saves PCB consumption.

➤ Applications

- Replace Digital Transistor
- Battery Operated Systems
- Power Supply Converter Circuits
- Load/Power Switching cell Phones

➤ Ordering Information

Device	Package	Shipping
SSC8132GN1	DFN1006	10K/Reel



Marking



➤ **Absolute Maximum Ratings**($T_A=25^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain-to-Source Voltage	35	V
V_{GSS}	Gate-to-Source Voltage	± 10	V
I_D	Continuous Drain Current ^a	2	A
I_{DM}	Pulsed Drain Current ^b	6	A
P_D	Power Dissipation ^c	2	W
T_J	Operation junction temperature	-55 to 150	$^{\circ}\text{C}$
T_{STG}	Storage temperature range	-55 to 150	$^{\circ}\text{C}$

➤ **Thermal Resistance Ratings**($T_A=25^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter	Maximum	Unit
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance ^a	60	$^{\circ}\text{C}/\text{W}$

Note:

- The value of $R_{\theta JA}$ is measured with the device mounted on 1 in² FR-4 board with 2oz.copper, in a still air environment with $T_A=25^{\circ}\text{C}$. The value in any given application depends on the user is specific board design. The current rating is based on the $t \leq 10\text{s}$ thermal resistance rating.
- Repetitive rating, pulse width limited by junction temperature.
- The power dissipation P_D is based on $T_{J(\text{MAX})}=150^{\circ}\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

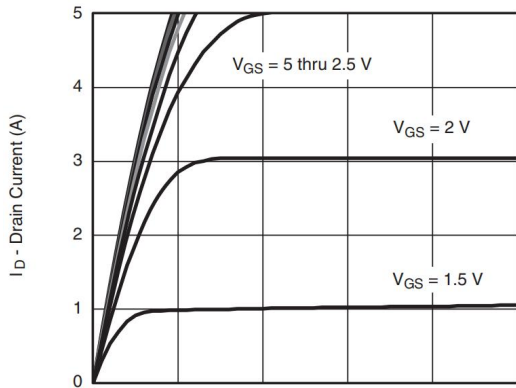


➤ **Electronics Characteristics**($T_A=25^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	35			V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	0.5	0.7	1	V
$R_{DS(on)}$	Drain-Source On-Resistance	$V_{GS}=4.5V, I_D=0.5A$		320	550	mR
		$V_{GS}=2.5V, I_D=0.3A$		350	750	
		$V_{GS}=1.8V, I_D=0.1A$		430	950	
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=24V, V_{GS}=0V$			1	μA
I_{GSS}	Gate-Source leak current	$V_{GS}=\pm 10V, V_{DS}=0V$			± 10	μA
G_{FS}	Transconductance	$V_{DS}=5V, I_D=2A$		2		S
V_{SD}	Forward Voltage	$V_{GS}=0V, I_S=0.5A$		0.8	1.3	V
C_{iss}	Input Capacitance	$V_{DS}=15V, V_{GS}=0V, f=1MHz$		44		pF
C_{oss}	Output Capacitance			11		
C_{rss}	Reverse Capacitance			6		
$T_{D(ON)}$	Turn-on delay time	$V_{GS}=4.5V,$ $V_{DS}=15V, R_L=2.3R$ $R_G=3R$		13		ns
T_r	Rise time			6.2		
$T_{D(OFF)}$	Turn-off delay time			2.8		
T_f	Fall time			5.6		
Q_g	Total Gate charge	$V_{GS}=4.5V, V_{DS}=10V$ $I_D=2A$		0.8		nC
Q_{gs}	Gate Source charge			0.1		
Q_{gd}	Gate Drain charge			0.2		

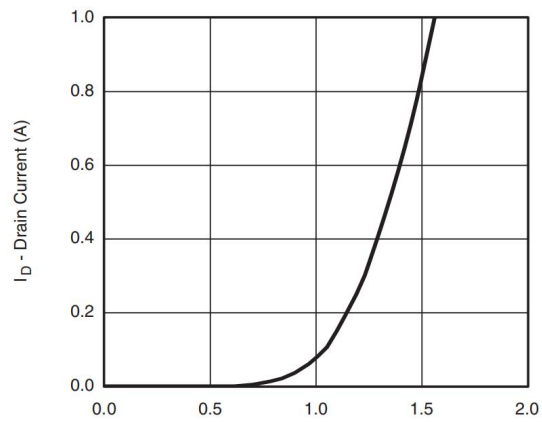


➤ **Typical Characteristics** ($T_A=25^\circ\text{C}$ unless otherwise noted)



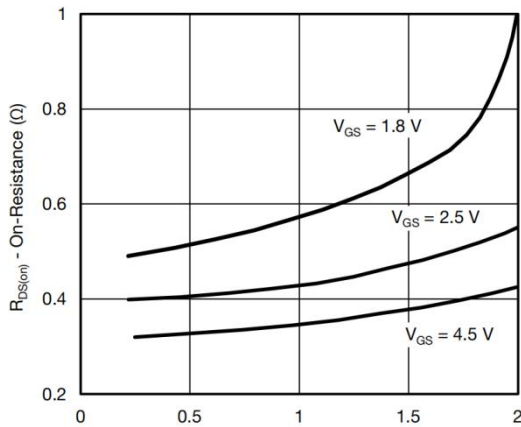
V_{DS} - Drain-to-Source Voltage (V)

Output Characteristics



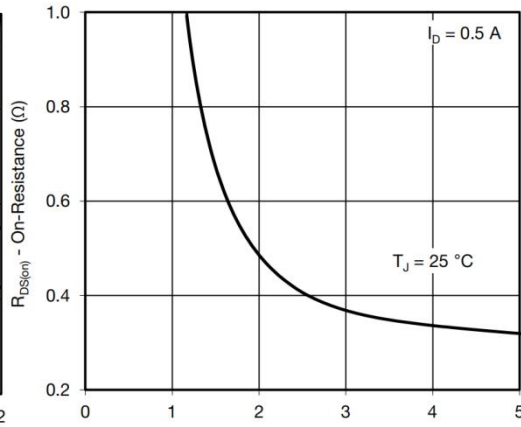
V_{GS} - Gate-to-Source Voltage (V)

Transfer Characteristics



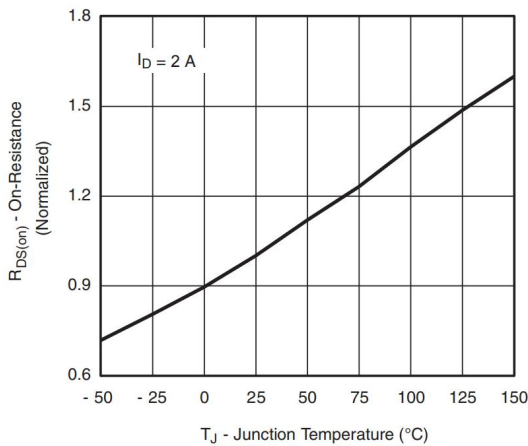
I_D - Drain Current (A)

On-Resistance vs. Drain Current

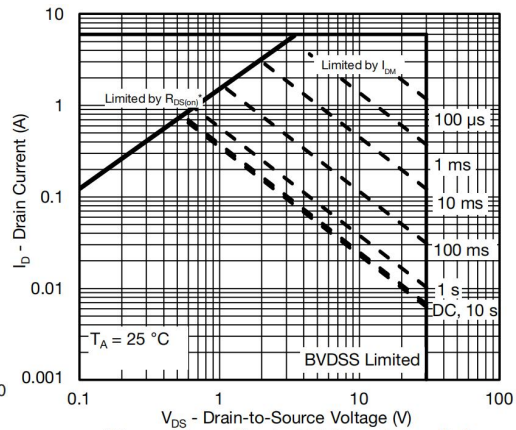


V_{GS} - Gate-to-Source Voltage (V)

On-Resistance vs. Gate-to-Source Voltage



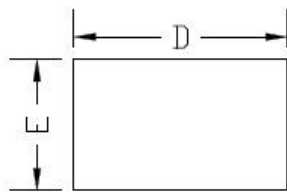
On-Resistance vs. Junction Temperature



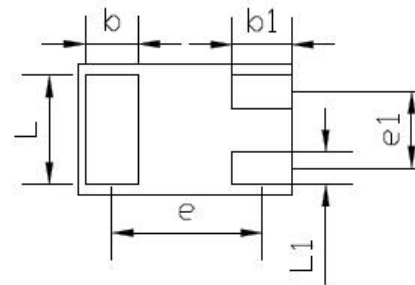
Safe Operating Area, Junction-to-Ambient

➤ Package Information

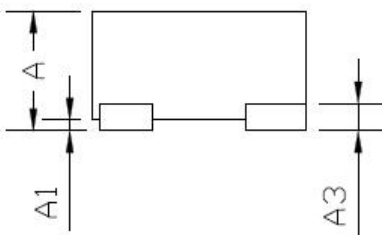
DFN1006-3L



TOP VIEW

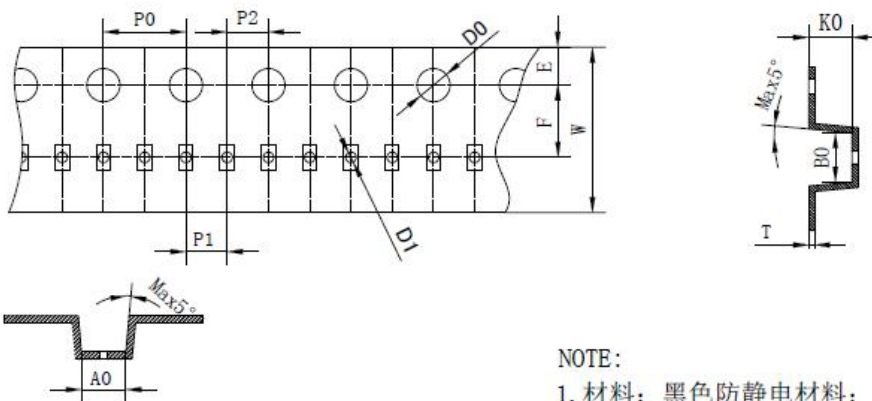


BOTTOM VIEW



SIDE VIEW

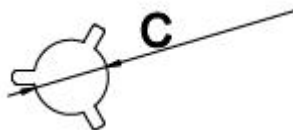
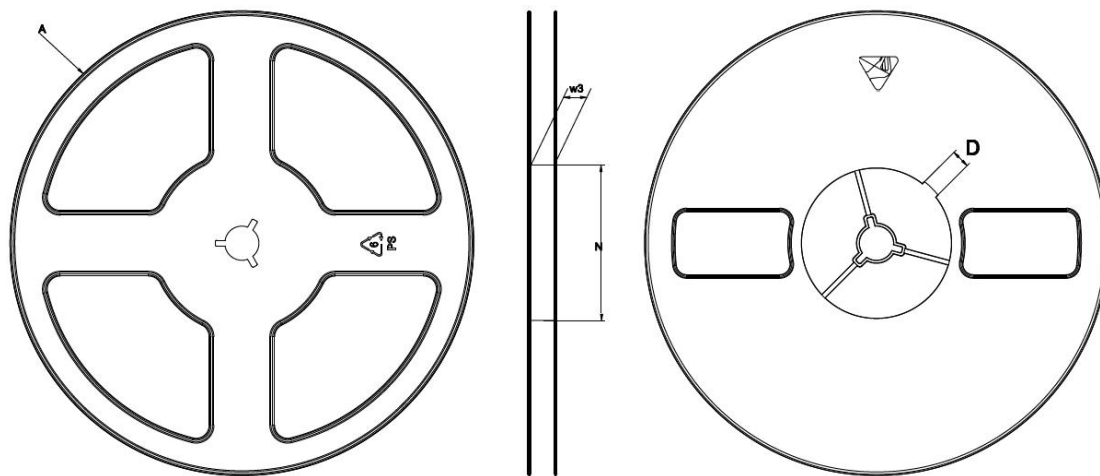
COMMON DIMENSION (MM)			
PKG	DFN1006		
REF.	MIN.	NOM.	MAX
A	>0.4	-	0.50
A1	0.00	-	0.05
A3	0.125REF.		
D	0.95	1.00	1.05
E	0.55	0.60	0.65
b	0.20	0.25	0.30
b1	0.20	0.30	0.40
L	0.45	0.50	0.55
L1	0.10	0.15	0.20
e	0.675		
e1	0.35		

Tape Data

NOTE:

1. 材料：黑色防静电材料；
2. 10个链孔的累积公差不能超过 ± 0.2
3. 尺寸符合EIA-481-E的要求。

SYMBOL	A0	B0	K0	P0	P1	P2
SPEC	0.69 \pm 0.05	1.15 \pm 0.05	0.60 \pm 0.05	4.00 \pm 0.10	2.00 \pm 0.05	2.00 \pm 0.05
SYMBOL	T	E	F	D0	D1	W
SPEC	0.18 \pm 0.03	1.75 \pm 0.10	3.50 \pm 0.05	1.55 \pm 0.05	0.50 \pm 0.05	8.00 ^{+0.3} _{-0.1}

Reel Data



材质说明: 该产品用料为 PS

TYPE	A	N	C	D	w3
8MM	$\begin{matrix} +1 \\ \text{Ø178} \\ -1 \end{matrix}$	$\begin{matrix} +1 \\ \text{Ø60} \\ -1 \end{matrix}$	$\begin{matrix} +0,3 \\ \text{Ø13,3} \\ -0,3 \end{matrix}$	$7,5 \pm 0,5$	$9 \pm 0,3$

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