



SSC8329GSB

Dual P-Channel Enhancement Mode MOSFET

➤ Features

V _{DS}	V _{GS}	R _{DS(ON)} Typ.	I _D
-20V	±12V	36mΩ@-4V5	-4.5A
		56mΩ@-2V5	
		89mΩ@-1V8	

➤ Description

This device is from Advanced Power innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

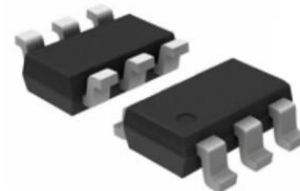
➤ Applications

- Load Switch
- Video monitor
- Power management
- DCDC conversion

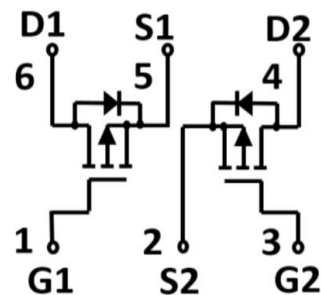
➤ Ordering Information

Device	Package	Shipping
SSC8329GSB	SOT-23-6L	3000/Reel

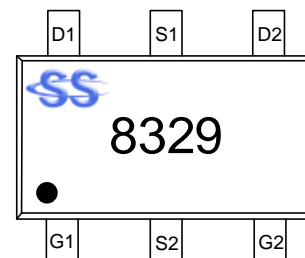
➤ Pin configuration



SOT-23-6L



Pin Configuration



Marking (Top View)



➤ **Absolute Maximum Ratings ($T_A=25^{\circ}\text{C}$ unless otherwise noted)**

Parameter		Symbol	Ratings	Unit
Drain-to-Source Voltage		V_{DSS}	-20	V
Gate-to-Source Voltage		V_{GSS}	± 12	V
Continuous Drain Current ^a	$T_C=25^{\circ}\text{C}$	I_D	-4.5	A
	$T_C=100^{\circ}\text{C}$		-2.5	
Pulsed Drain Current ^b		I_{DM}	-17.9	A
Power Dissipation ^c	$T_C=25^{\circ}\text{C}$	P_D	1.1	W
	$T_C=100^{\circ}\text{C}$		0.43	
Operation junction temperature		T_J	-55~150	$^{\circ}\text{C}$
Storage temperature range		T_{STG}	-55~150	

➤ **Thermal Resistance Ratings ($T_A=25^{\circ}\text{C}$ unless otherwise noted)**

Parameter	Symbol	Typical	Maximum	Unit
Junction-to-Ambient Thermal Resistance ^a	$R_{\theta JA}$		115	$^{\circ}\text{C}/\text{W}$

Note:

- The value of $R_{\theta JA}$ is measured with the device mounted on 1 in² FR-4 board with 2oz.copper, in a still air environment with $T_A=25^{\circ}\text{C}$. The value in any given application depends on the user's specific board design. The current rating is based on the $t \leq 10\text{s}$ thermal resistance rating.
- Repetitive rating, pulse width limited by junction temperature.
- The power dissipation P_D is based on $T_{J(MAX)}=150^{\circ}\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

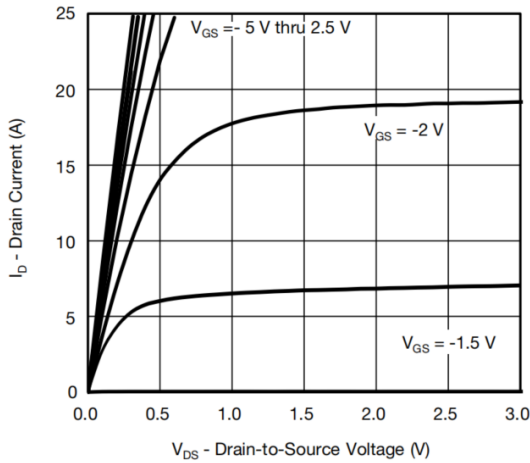


➤ **Electrical Characteristics (T_A=25°C unless otherwise noted)**

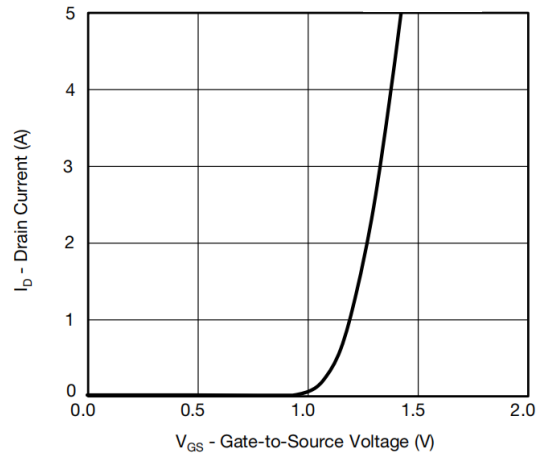
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = -250μA	-20			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250μA	-0.4	-0.7	-1	V
Drain-Source On-Resistance	R _{DS(on)}	V _{GS} = -4.5V, I _D = -3A		36	48	mΩ
		V _{GS} = -2.5V, I _D = -2A		56	68	
		V _{GS} = -1.8V, I _D = -1A		89	125	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -16V, V _{GS} = 0V			-1	μA
Gate-Source Leak Current	I _{GSS}	V _{GS} = ±12V, V _{DS} = 0V			±100	nA
Forward Voltage	V _{SD}	V _{GS} = 0V, I _S = -2A			-1.3	V
Input Capacitance	C _{ISS}	V _{GS} = 0V, V _{DS} = -10V, f = 1MHz		580		pF
Output Capacitance	C _{OSS}			71		
Reverse Transfer Capacitance	C _{RSS}			56		
Total Gate Charge	Q _G	V _{GS} = -4.5V, V _{DS} = -10V, I _D = -2A		6		nC
Gate to Source Charge	Q _{GS}			1		
Gate to Drain Charge	Q _{GD}			1.2		
Turn-on Delay Time	T _{D(ON)}	V _{GS} = -4.5V, V _{DS} = -10V, I _D = -2A, R _G = 3Ω		5.8		ns
Rise Time	T _r			23		
Turn-off Delay Time	T _{D(OFF)}			102		
Fall Time	T _f			245		
Diode Recovery Time	T _{rr}	I _F = -2A, di/dt = 50A/us		38		ns
Diode Recovery Charge	Q _{rr}			4.7		nC



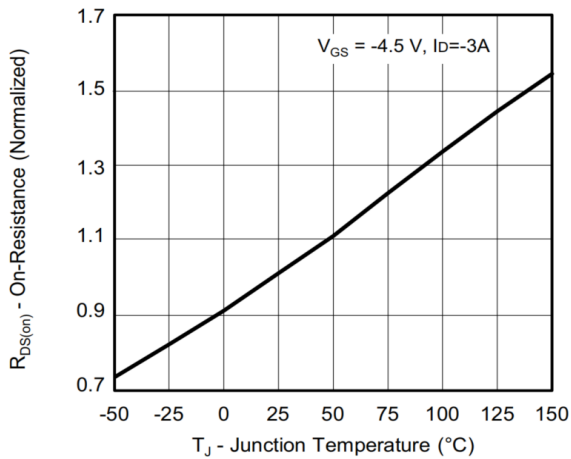
➤ Typical Performance Characteristics (T_A=25°C unless otherwise noted)



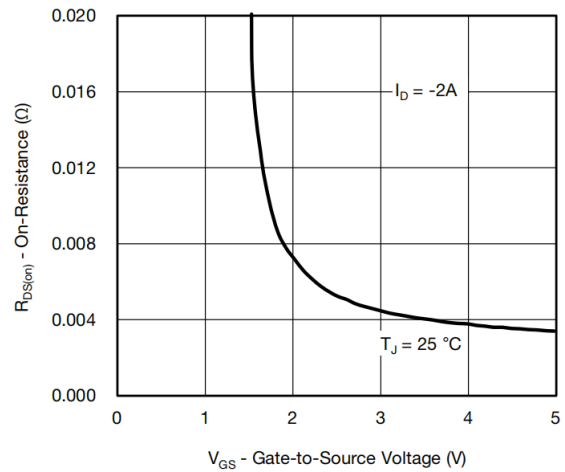
Output Characteristics



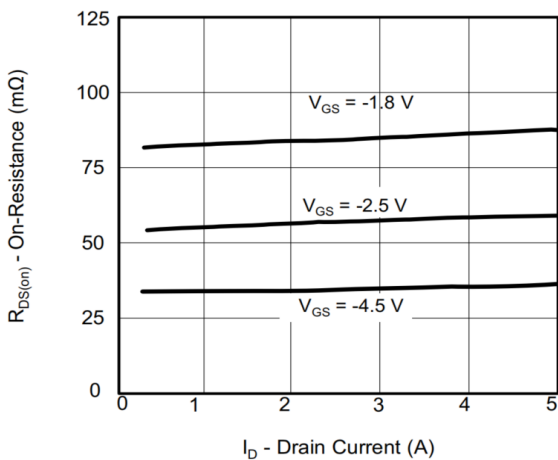
Transfer Characteristics



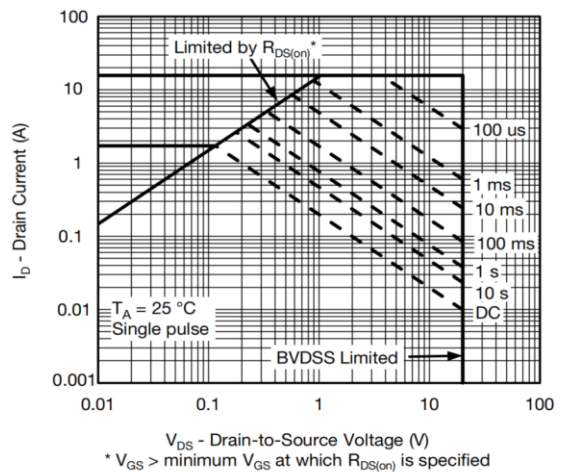
On-Resistance vs. Junction Temperature



On-Resistance vs. Gate-to-Source Voltage



On-Resistance vs. Drain Current and Gate Voltage

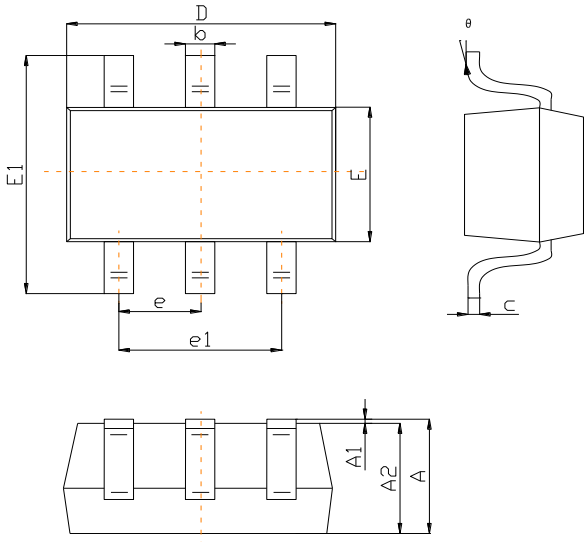


Safe Operating Area, Junction-to-Ambient



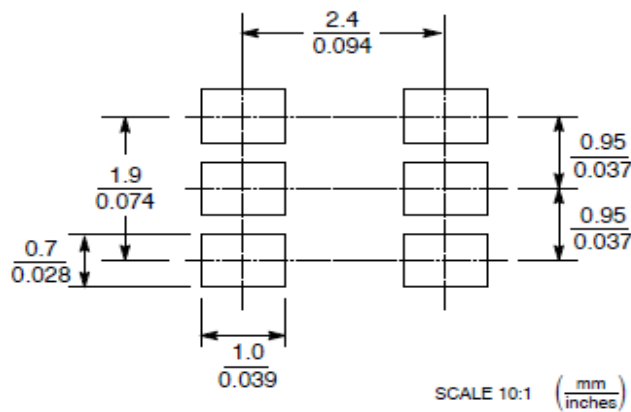
➤ **Package Information**

● **Mechanical Data**



DIM	Millimeters		
	MIN	NOM	MAX
A	1.100	1.150	1.250
A1	0.020	0.060	0.100
A2	1.050	1.100	1.150
b	0.320	0.350	0.480
c	0.152REF		
D	2.870	2.920	2.970
E	1.550	1.600	1.650
E1	2.600	2.800	3.000
e	0.950(BSC)		
e1	1.800	1.900	2.000
L	0.350	0.450	0.550
θ	0	3°	7°

● **Recommended Pad outline**





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