



## SSC8166GN2

### N-Channel Enhancement Mode MOSFET

#### ➤ Features

V <sub>DS</sub>	V <sub>GS</sub>	R <sub>DS(ON)</sub> Typ.	I <sub>D</sub>
60V	±20V	32mΩ@10V	7A
		35mΩ@4V5	

#### ➤ Description

This device is produced with high cell density DMOS trench technology, which is especially used to minimize on-state resistance. This device particularly suits low voltage applications such as portable equipment, power management and other battery powered circuits, and low in-line power dissipation are needed in a very small outline surface mount package.

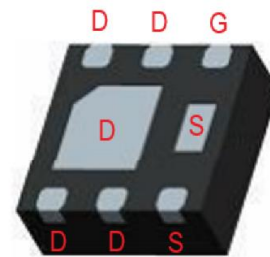
#### ➤ Applications

- Load Switch
- Portable Devices
- DCDC Conversion
- Charging

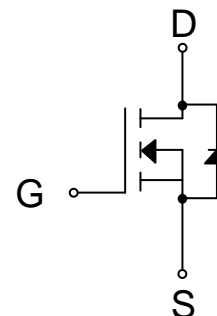
#### ➤ Ordering Information

Device	Package	Shipping
SSC8166GN2	DFN2020-6L	3000/Reel

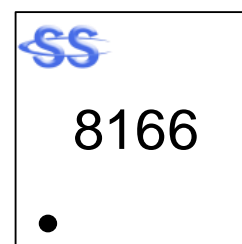
#### ➤ Pin Configuration



**DFN2020-6L (Bottom View)**



**Pin Configuration**



**Marking**



➤ **Absolute Maximum Ratings ( $T_A=25^{\circ}\text{C}$  unless otherwise noted)**

Parameter		Symbol	Ratings	Unit
Drain-to-Source Voltage		$V_{DS}$	60	V
Gate-to-Source Voltage		$V_{GS}$	$\pm 20$	V
Continuous Drain Current <sup>d</sup>	$T_C=25^{\circ}\text{C}$	$I_D$	7	A
	$T_C=100^{\circ}\text{C}$		4	
Pulsed Drain Current <sup>b</sup>		$I_{DM}$	30	A
Power Dissipation <sup>c</sup>	$T_C=25^{\circ}\text{C}$	$P_D$	3.1	W
	$T_C=100^{\circ}\text{C}$		1.25	
Operation junction temperature		$T_J$	-55~150	$^{\circ}\text{C}$
Storage temperature range		$T_{STG}$	-55~150	

➤ **Thermal Resistance Ratings ( $T_A=25^{\circ}\text{C}$  unless otherwise noted)**

Parameter	Symbol	Maximum	Unit
Junction-to-Ambient Thermal Resistance <sup>a</sup>	$R_{\theta JA}$	40	$^{\circ}\text{C}/\text{W}$

Note:

- The value of  $R_{\theta JA}$  is measured with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz.copper, in a still air environment with  $T_A=25^{\circ}\text{C}$ . The value in any given application depends on the user is specific board design. The power dissipation is based on the  $t \leq 10\text{s}$  thermal resistance rating.
- Repetitive rating, pulse width limited by junction temperature.
- The power dissipation  $P_D$  is based on  $T_{J(MAX)}=150^{\circ}\text{C}$ , using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.
- The maximum current rating is package limited.

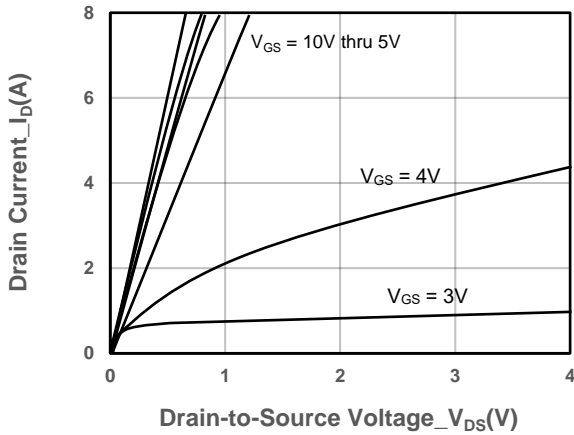


➤ **Electrical Characteristics (T<sub>A</sub>=25°C unless otherwise noted)**

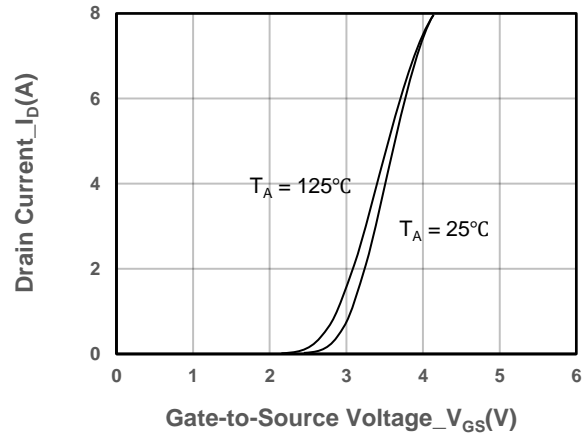
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250uA	60			V
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250uA	1	1.5	2.5	V
Drain-Source On-Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10V, I <sub>D</sub> = 6A		32	37	mΩ
		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 3A		35	43	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 60V, V <sub>GS</sub> = 0V			1	μA
Gate-Source Leak Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20V, V <sub>DS</sub> = 0V			±100	nA
Forward Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0V, I <sub>S</sub> = 2A		0.75	1.3	V
Input Capacitance	C <sub>ISS</sub>	V <sub>DS</sub> = 15V, V <sub>GS</sub> = 0V, f = 1MHz		1210		pF
Output Capacitance	C <sub>OSS</sub>			65		
Reverse Transfer Capacitance	C <sub>RSS</sub>			53		
Total Gate Charge	Q <sub>G</sub>	V <sub>GS</sub> = 4.5V, V <sub>DS</sub> = 15V, I <sub>D</sub> = 5A		9		nC
Gate to Source Charge	Q <sub>GS</sub>			3.1		
Gate to Drain Charge	Q <sub>GD</sub>			3		
Turn-on Delay Time	T <sub>D(ON)</sub>	V <sub>GS</sub> = 4.5V, V <sub>DS</sub> = 10V, R <sub>L</sub> = 1.4Ω, R <sub>G</sub> = 6Ω, I <sub>D</sub> = 5A		6		ns
Rise Time	T <sub>r</sub>			6		
Turn-off Delay Time	T <sub>D(OFF)</sub>			32		
Fall Time	T <sub>f</sub>			11		



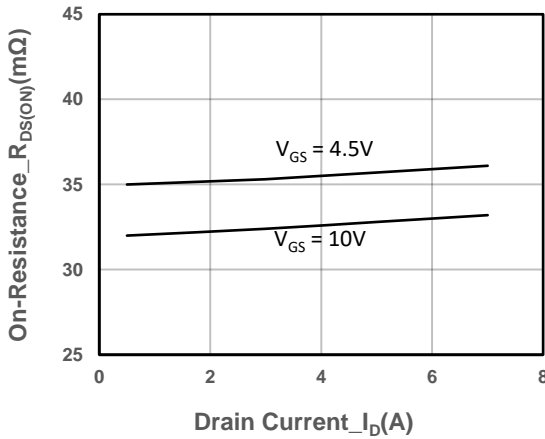
➤ **Typical Performance Characteristics ( $T_A=25^\circ\text{C}$  unless otherwise noted)**



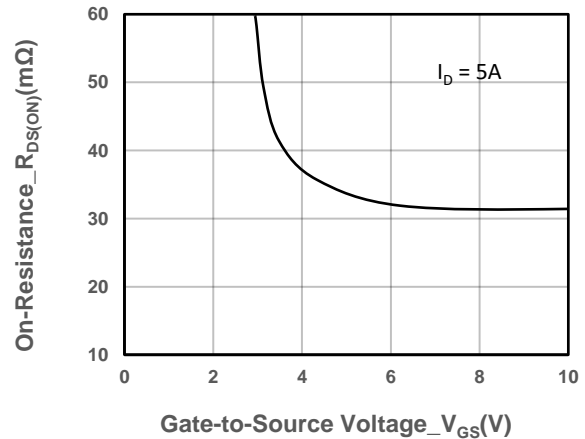
**Output Characteristics**



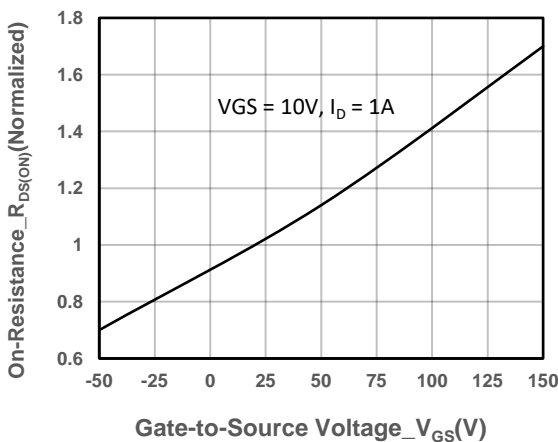
**Transfer Characteristics**



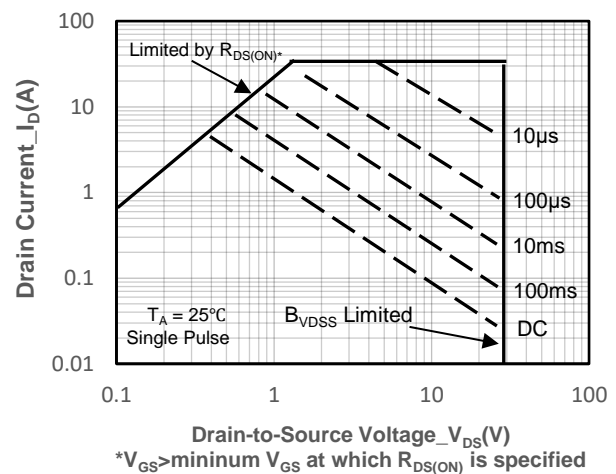
**On-Resistance vs. Drain Current and Gate Voltage**



**On-Resistance vs. Gate-to-Source Voltage**



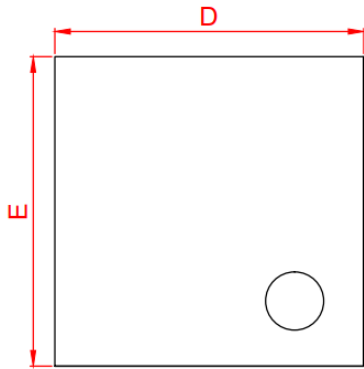
**On-Resistance vs. Junction Temperature**



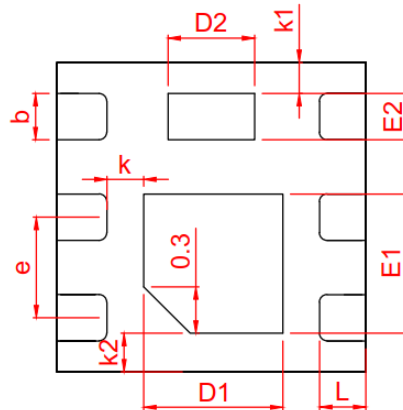
**Safe Operating Area vs. Junction-to-Ambient**



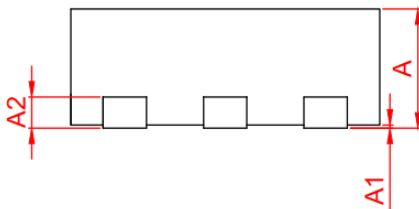
## ➤ Package Information



TOP VIEW



BOTTOM VIEW



SIDE VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.50	0.55	0.60
* A1	0.00	0.02	0.05
* b	0.25	0.30	0.35
* A2	0.152 BSC		
* D	1.95	2.00	2.05
* E	1.95	2.00	2.05
* E1	0.80	0.90	1.00
* E2	0.25	0.30	0.35
* D1	0.80	0.90	1.00
* D2	0.46	0.56	0.66
* e	0.65 REF		
* L	0.25	0.30	0.35
* K	0.20	0.25	0.30
* K1	0.15	0.20	0.25
* K2	0.20	0.25	0.30

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