

SSC8129GN4

P-Channel Enhancement Mode MOSFET

Features

V _{DS}	V _{GS}	R _{DS(ON)}	l _D
-20V	+12V	8mΩ@-4V5	- Λ 2Δ
-20 V	12 V	13mΩ@-2V5	-42A

> Description

This SSC8129GN4 uses advanced trench technology to provide excellent RDSON and low gate charge. The complementary MOSFETS may be used to form a level shifted high side switch, and for a host of other applications.

100% UIS + ΔVDS + Rg Tested!

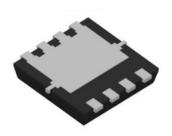
Applications

- Load Switch
- PWM Application
- Power Management
- Electronic Cigarette

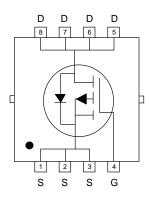
> Ordering Information

Device	Package	Shipping
SSC8129GN4	PDFN3.3X3.3-8L	5000/Reel

Pin configuration



PDFN3.3X3.3-8L (Bottom View)



Pin Configuration (Top View)



Marking

(YW: Internal Traceability Code)



➤ Absolute Maximum Ratings (T_A=25°C unless otherwise noted)

Symbol	Parameter	Ratings	Unit		
V _{DSS}	Drain-to-Source Volta	Drain-to-Source Voltage		V	
V _{GSS}	Gate-to-Source Volta	ge	±12	V	
		T _C =25℃	-42	Δ.	
I _D	Continuous Drain Current d	T _C =100°C	-22	Α	
	Continuous Busin Comment 2	T _A =25℃	-16	Δ.	
IDSM	Continuous Drain Current ^a	T _A =70°C	-12.5	- A	
I _{DM}	Pulsed Drain Curren	Pulsed Drain Current b		Α	
Б		Tc=25℃	23	10/	
P _D	Power Dissipation ^c	T _C =100°C	9	W	
Б	Dawer Dissipation 2	T _A =25℃	3.9	10/	
P _{DSM}	Power Dissipation ^a	T _A =70°C	2.5	W	
I _{AS}	Avalanche Current b L=0.5mH Single Pulse		-14	Α	
Eas	Avalanche Energy ^b L=0.5mH Single Pulse		49	mJ	
TJ	Operation junction temperature		-55~150	°C	
T _{STG}	Storage temperature range		-55~150	$^{\circ}$	

➤ Thermal Resistance Ratings (T_A=25°C unless otherwise noted)

Symbol	Parameter	Maximum	Unit
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance a	33	°C/W
R ₀ JC	Junction-to-Case Thermal Resistance	5.4	C/ VV

Note:

- a. The value of R_{θJA} is measured with the device mounted on 1 in² FR-4 board with 2oz.copper, in a still air environment with T_A=25 °C. The value in any given application depends on the user is specific board design. The power dissipation is based on the t≤10s thermal resistance rating.
- b. Repetitive rating, pulse width limited by junction temperature.
- c. The power dissipation P_D is based on $T_{J(MAX)}$ =150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.
- d. The maximum current rating is package limited.

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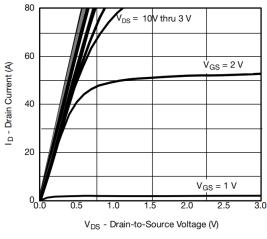


\succ Electrical Characteristics (T_A=25°C unless otherwise noted)

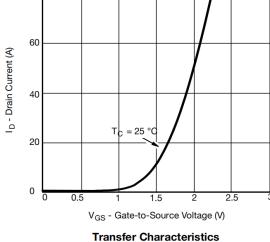
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Drain-Source Breakdown Voltage	V _{(BR)DSS}	$V_{GS} = 0V, I_{D} = -250\mu A$	-20			٧
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_{D} = -250uA$	-0.5	-0.75	-1	٧
Drain-Source On-Resistance	D	$V_{GS} = -4.5V, I_D = -10A$		8	12	mΩ
Diam-Source On-Resistance	R _{DS(on)}	V _{GS} = -2.5V, I _D = -7A		13	16	11177
Zero Gate Voltage Drain Current	IDSS	V _{DS} = -20V, V _{GS} = 0V			1	μA
Gate-Source Leak Current	Igss	$V_{GS} = \pm 12V$, $V_{DS} = 0V$			±100	nA
Transconductance	G _{FS}	V _{DS} = -5V, I _D = -10A		18		s
Forward Voltage	V _{SD}	V _{GS} = 0V, I _S = -2.3A		-0.7	-1.3	V
Gate Resistance	R _G	V _{DS} = 0V, f = 1MHz		9		Ω
Input Capacitance	Ciss	\/ 45\/\\ 0\/		3321		
Output Capacitance	Coss	$V_{DS} = -15V$, $V_{GS} = 0V$, $f = 1MHz$		365		pF
Reverse Transfer Capacitance	C _{RSS}	I = IIVIDZ		328		
Total Gate Charge	Q _G	\		16		
Gate to Source Charge	Q _{GS}	$V_{GS} = -4.5V, V_{DS} = -10V,$ $I_{D} = -7A$		2.4		nC
Gate to Drain Charge	Q _{GD}	ID = -/A		5.5		
Turn-on Delay Time	T _{D(ON)}			17		
Rise Time	Tr	V _{GS} = -4.5V, V _{DS} = -10V,		28		
Turn-off Delay Time	T _{D(OFF)}	$R_L = 1.5\Omega, R_G = 3\Omega$		72		ns
Fall Time	Tf			35		

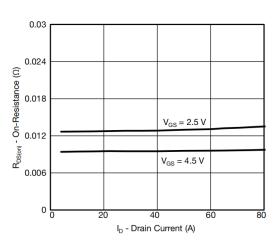


Typical Performance Characteristics (T_A=25℃ unless otherwise noted)

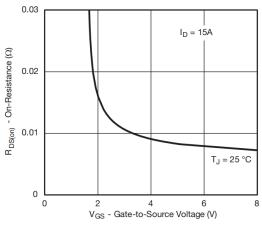


Output Characteristics

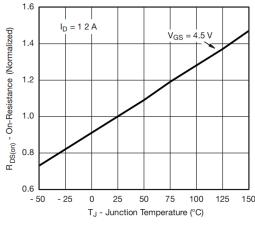




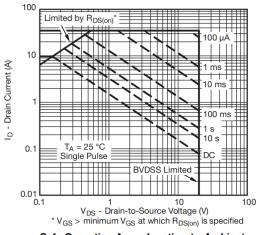
On-Resistance vs. Drain Current



On-Resistance vs. Gate-to-Source Voltage



On-Resistance vs. Junction Temperature

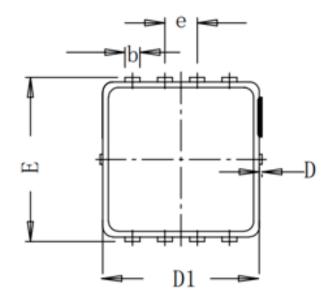


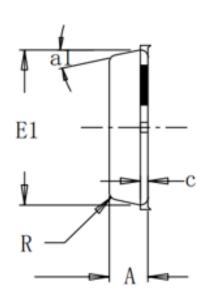
Safe Operating Area, Junction-to-Ambient

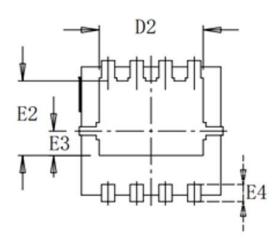
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> Package Information







Cumbal	Dimensions In Millimeters			
Symbol	Min.	Nom.	Max.	
Α	0.75	0.78	0.81	
b	0.297	0.3	0.35	
С	-	0.152	-	
D	0	0.05	0.1	
D1	3.12	3.15	3.18	
D2	-	2.35	-	
Е	3.2	3.3	3.4	
E1	3.09	3.12	3.15	
E2	-	1.75	-	
E3	-	0.575	-	
E4	-	0.4	-	
R	-	0.15	-	
е	0.65BSC			
a1°	-	12°	-	



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