SSC8162GS6

N-Channel Small Switching MOSFET with ESD Protection

➢ Features

V_{DS}	V_{GS}	$R_{DS(ON)}$ Typ.	I_D	ESD
60V	$\pm$12V	1Ω@10V	0.5A	500V
		1.5Ω@4V5		

➢ Description

This device is an N-Channel enhancement mode MOSFET which is produced with high cell density and DMOS trench technology. This device particularly suits low voltage applications, especially for battery powered circuits, the tiny and thin outline saves PCB consumption.
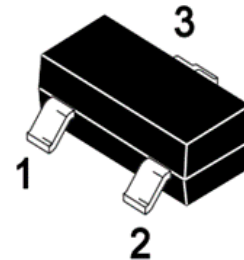
➢ Applications

● Direct Logic-Level Interface: TTL/CMOS

● Drivers: Relays, Solenoids, Lamps, Hammers

● Display, Memories, Transistors, etc.
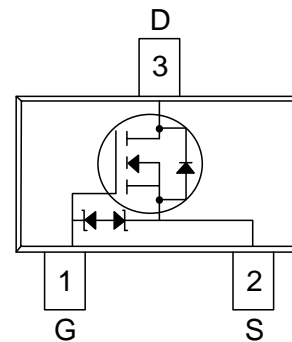
● Battery Operated System

● Solid-State Relays

➢ Ordering Information

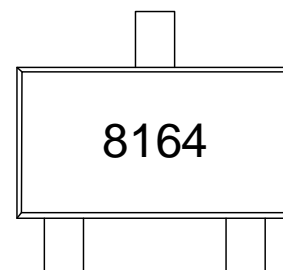| Device	Package	Shipping
SSC8162GS6	SOT-23	3000/Reel

➢ Pin configuration

SOT-23

Pin Configuration (Top View)

Marking

➢ Absolute Maximum Ratings (T$_A$=25℃ unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V$_{DSS}$	Drain-to-Source Voltage	60	V
V$_{GSS}$	Gate-to-Source Voltage	±12	V
I$_D$	Continuous Drain Current [a]	0.5	A
I$_{DM}$	Pulsed Drain Current [b]	1	A
P$_D$	Power Dissipation [c]	0.85	W
P$_{DSM}$	Power Dissipation [a]	0.36	W
T$_J$	Operation junction temperature	-55~150	℃
T$_{STG}$	Storage temperature range	-55~150	℃

➢ Thermal Resistance Ratings (T$_A$=25℃ unless otherwise noted)

Symbol	Parameter	Maximum	Unit
R$_{θJA}$	Junction-to-Ambient Thermal Resistance [a]	360	℃/W
R$_{θJC}$	Junction-to-Case Thermal Resistance	155	℃/W

Note:

a. The value of R$_{θJA}$ is measured with the device mounted on 1 in^2 FR-4 board with 2oz.copper, in a still air environment with T$_A$=25℃.The value in any given application depends on the user is specific board design. The power dissipation is based on the t≤10s thermal resistance rating.

b. Repetitive rating, pulse width limited by junction temperature.

c. The power dissipation P$_D$ is based on T$_{J(MAX)}$=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

## ➢ Electrical Characteristics (T_A=25℃ unless otherwise noted)

| Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	60			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250uA	0.75	1	1.25	V
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = 10V, I_D = 0.5A		1.1	2.5	Ω
		V_{GS} = 4.5V, I_D = 0.5A		1.5	3.5	
		V_{GS} = 2.5V, I_D = 0.2A		1.7	4	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 60V, V_{GS} = 0V			1	μA
Gate-Source Leak Current	I_{GSS}	V_{GS} = ±12V, V_{DS} = 0V			±10	μA
Transconductance	G_{FS}	V_{DS} = 10V, I_D = 0.2A		0.1		s
Forward Voltage	V_{SD}	V_{GS} = 0V, I_S = 0.2A			1.3	V
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz		32		pF
Output Capacitance	C_{OSS}			6.3		
Reverse Transfer Capacitance	C_{RSS}			2.9		
Turn-on Delay Time	$T_{D(ON)}$	V_{GS} = 10V, V_{DS} = 10V, I_D = 0.1A		26		ns
Rise Time	T_r			10.5		
Turn-off Delay Time	$T_{D(OFF)}$			37		
Fall Time	T_f			21		
Total Gate Charge	Q_G	V_{GS} = 10V, V_{DS} = 15V, I_D = 0.2A		0.4		nC
Gate to Source Charge	Q_{GS}			0.1		
Gate to Drain Charge	Q_{GD}			0.11		

➢ **Typical Performance Characteristics (T$_A$=25℃ unless otherwise noted)**
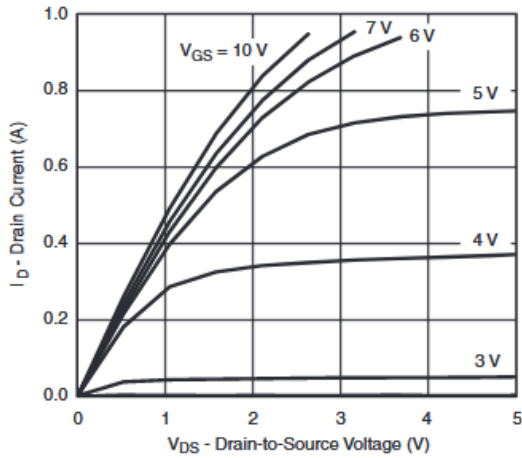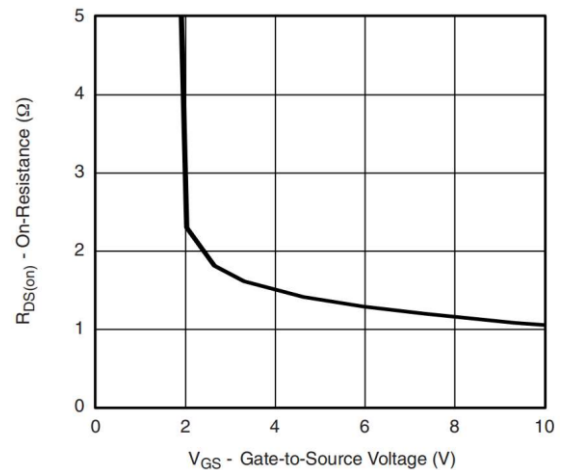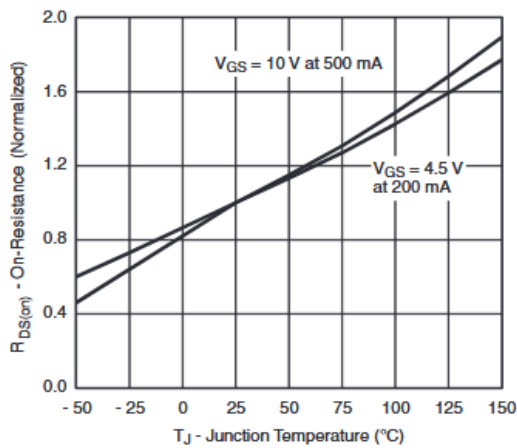

Output Characteristics
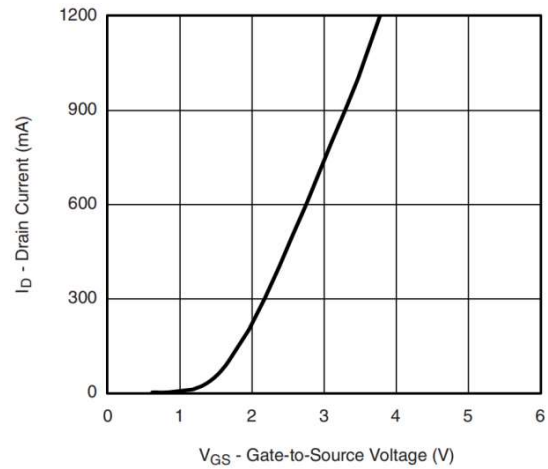
Transfer Characteristics
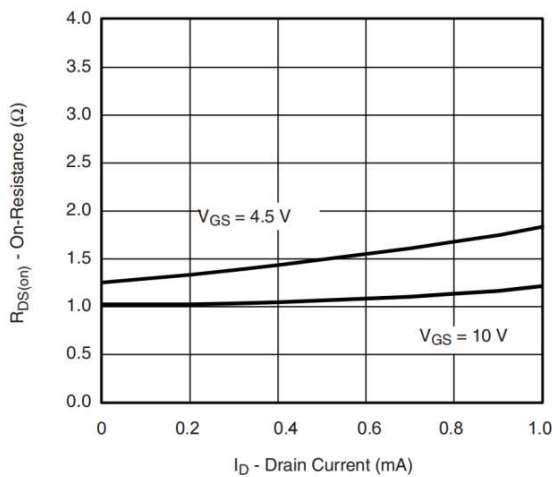
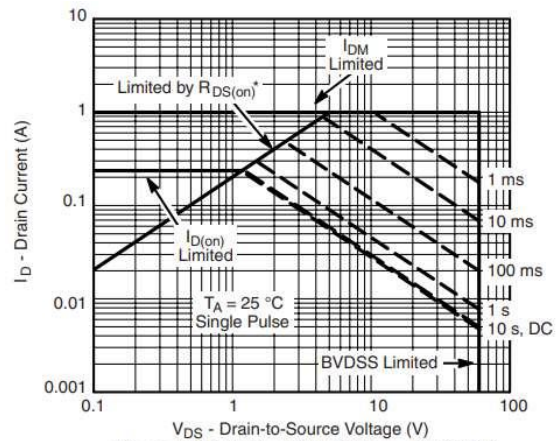
On-Resistance vs. Drain Current

On-Resistance vs. Gate-Source Voltage

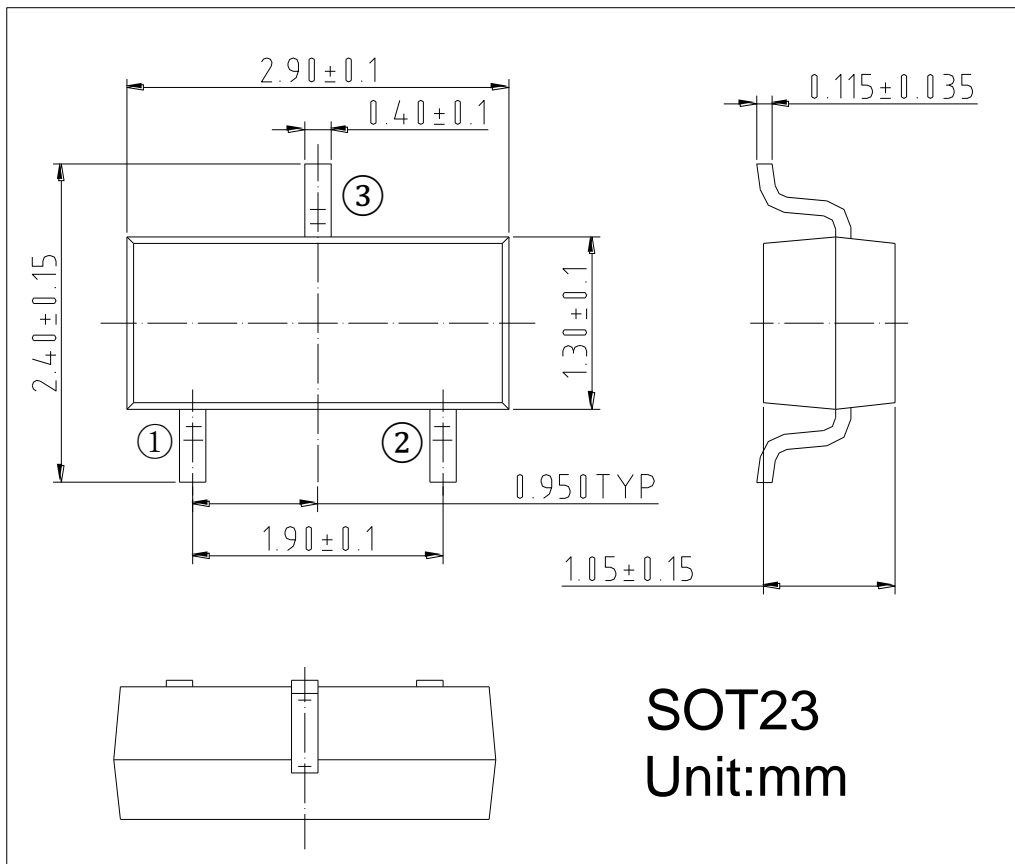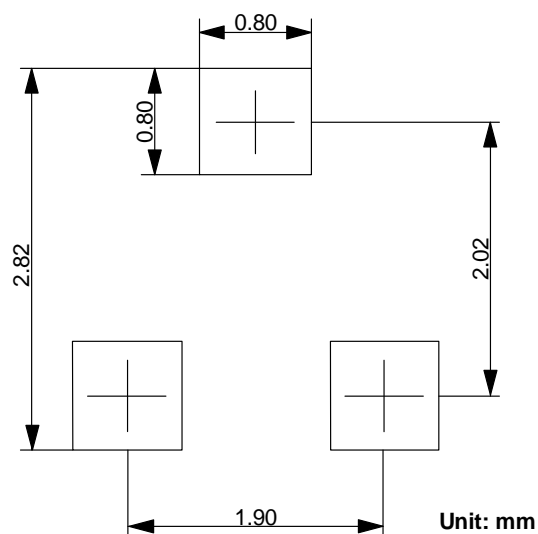**On-Resistance vs. Junction Temperature**

Safe Operating Area

➢ **Package Information**

SOT23
Unit:mm

➢ **Suggested Pad Layout**

Unit: mm

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