# SSC8326GS1

## Dual N-Channel Enhancement Mode MOSFET

### ➢ Features

| VDS | VGS | RDSON Typ. | ID |
|---|---|---|---|
| 20V | ±12V | 20mR@4V5 | 6A |
| | | 24mR@2V5 | |

### ➢ Description

This device is produced with high cell density, DMOS trench technology, which is especially used to minimize on-state resistance. This device is particularly suited for low voltage power management requiring a wild range of given voltage ratings(4.5V~25V) such as load switch and battery protection.

### ➢ Applications

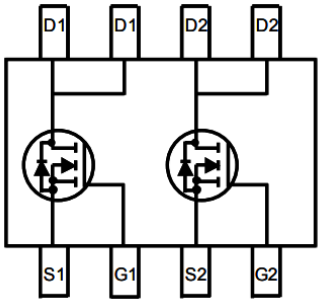
- Li Battery
- Battery charge
- Load Switch

### ➢ Ordering Information

| Device | Package | Shipping |
|---|---|---|
| SSC8326GS1 | SOP-8 | 4000/Reel |

### ➢ Pin configuration

Top view




Bottom View


Marking

## ➢ Absolute Maximum Ratings($T_A$=25℃ unless otherwise noted)

| Symbol | Parameter | Ratings | Unit |
|---|---|---|---|
| $V_{DSS}$ | Drain-to-Source Voltage | 20 | V |
| $V_{GSS}$ | Gate-to-Source Voltage | ±12 | V |
| $I_D$ | Continuous Drain Current [a] | 6 | A |
| $I_{DM}$ | Pulsed Drain Current [b] | 24 | A |
| $P_D$ | Power Dissipation [c] | 3.1 | W |
| $P_{DSM}$ | Power Dissipation [a] | 1.1 | W |
| $T_J$ | Operation junction temperature | -55 to 150 | ℃ |
| $T_{STG}$ | Storage temperature range | -55 to 150 | ℃ |

## ➢ Thermal Resistance Ratings($T_A$=25℃ unless otherwise noted)

| Symbol | Parameter | Typical | Maximum | Unit |
|---|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-Ambient Thermal Resistance [a] | | 120 | ℃/W |
| $R_{\theta JC}$ | Junction-to-Case Thermal Resistance | | 45 | |

Note:

a. The value of RθJA is measured with the device mounted on 1 $in^2$ FR-4 board with 2oz.copper,in a still air environment with TA=25℃.The value in any given application depends on the user is specific board design. The current rating is based on the t≤ 10s thermal resistance rating.

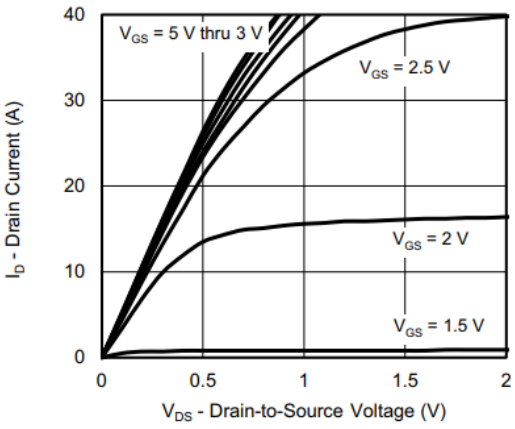
b. Repetitive rating, pulse width limited by junction temperature.

c. The power dissipation PD is based on TJ(MAX)=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

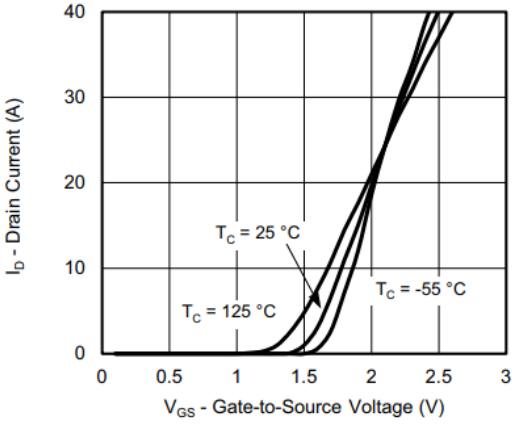
➢ **Electronics Characteristics**($T_A$=25℃ unless otherwise noted)

| Symbol | Parameter | Test Conditions | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-Source Breakdown Voltage | VGS=0V,ID=250uA | 20 | | | V |
| $V_{GS\ (th)}$ | Gate Threshold Voltage | VDS=VGS,ID=250uA | 0.5 | 0.7 | 1 | V |
| $R_{DS(on)}$ | Drain-Source On-Resistance | VGS=4.5V,ID=2A | | 20 | 24 | mR |
| | | VGS=2.5V,ID=2A | | 24 | 34 | |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | VDS=20V,VGS=0V | | | 1 | uA |
| $I_{GSS}$ | Gate-Source leak current | VGS=±12V,VDS=0V | | | ±100 | nA |
| $V_{SD}$ | Forward Voltage | VGS=0V,IS=1.7A | | 0.7 | 1.3 | V |
| $G_{FS}$ | Transconductance | VDS=10V , ID=4A | | 10 | | S |
| Ciss | Input Capacitance | VDS=10V, VGS=0V, f=1MHz | | 610 | | pF |
| Coss | Output Capacitance | | | 335 | | |
| Crss | Reverse Transfer Capacitance | | | 148 | | |
| $T_{D(ON)}$ | Turn-on delay time | VGS=4.5V, VDS=10V, RG=6R,ID=1A | | 8 | | ns |
| Tr | Rise time | | | 7 | | |
| $T_{D(OFF)}$ | Turn-off delay time | | | 35 | | |
| Tf | Fall time | | | 10 | | |
| Qg | Total Gate charge | VGS=4.5V , VDS=15V , ID=3A | | 10.5 | | nC |
| Qgs | Gate to Source charge | | | 1.9 | | |
| Qgd | Gate to Drain charge | | | 1.8 | | |

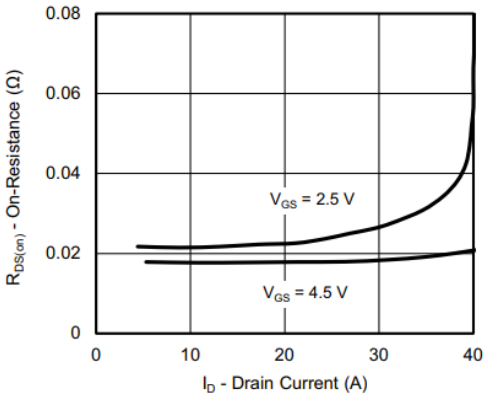
## ➢ Typical Characteristics($T_A$=25℃ unless otherwise noted)



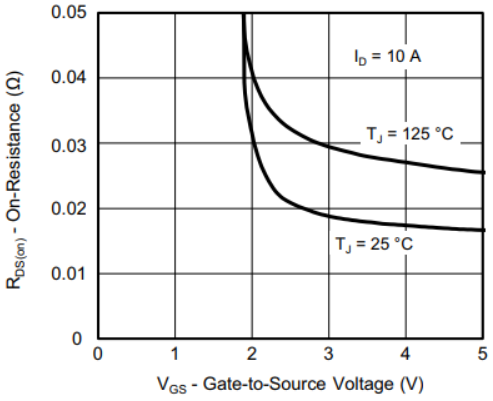

**Output Characteristics**



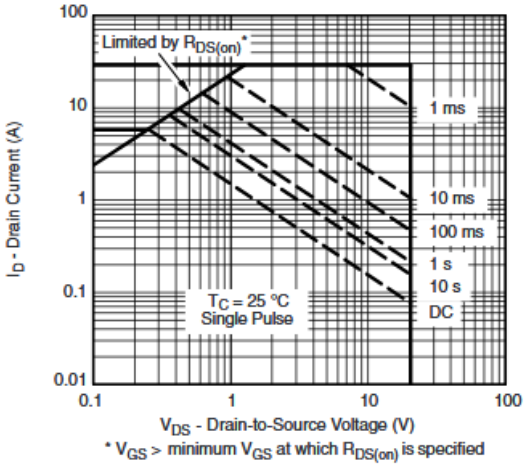

**Transfer Characteristics**



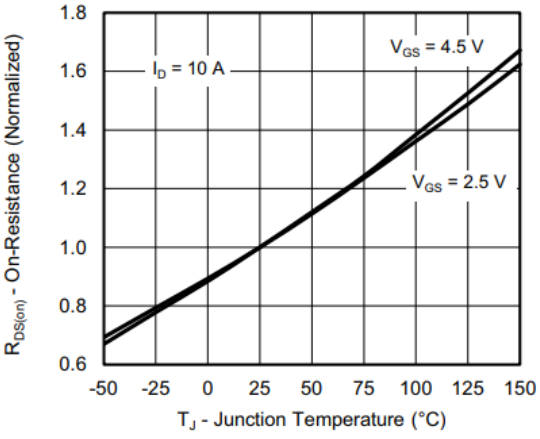

**On-Resistance vs. Drain Current and Gate Voltage**



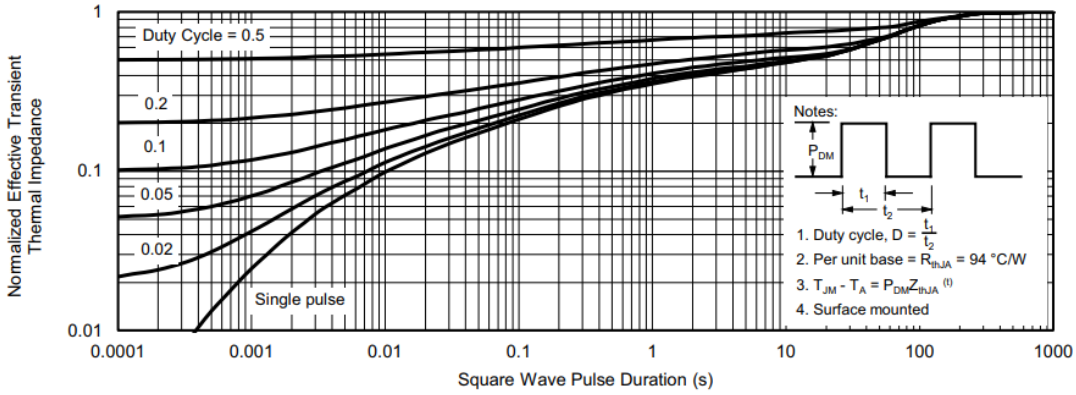

**On-Resistance vs. Gate-to-Source Voltage**




**Safe Operating Area, Junction-to-Case**

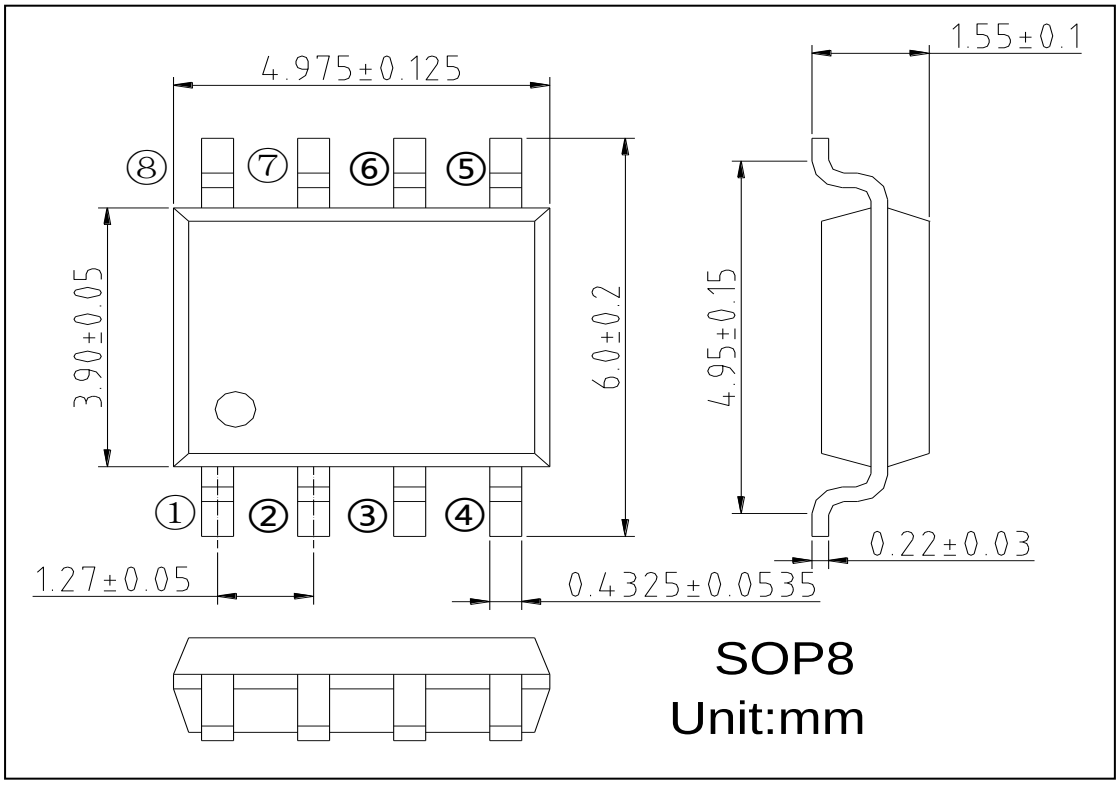



**On-Resistance vs. Junction Temperature**




**Normalized Thermal Transient Impedance, Junction-to-Ambient**

## ➢ Package Information

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