

SSC8120GS6

N-Channel Enhancement Mode MOSFET

Features

V _{DS}	V _{GS}	R _{DS(ON)} Typ.	I _D	ESD
		310mΩ@4V5		
20V	±12V	490mΩ@2V5	1.2A	1.2K
		850mΩ@1V8		

Description

This device is a N-Channel enhancement mode MOSFET which is produced with high cell density and DMOS trench technology. This device particularly suits low voltage applications, especially for battery powered circuits, the tiny and thin outline saves PCB consumption.

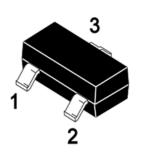
Applications

- Replace Digital Transistor
- Battery Operated Systems
- Power Supply Converter Circuits
- Load/Power Switching Cell Phones

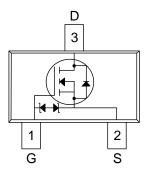
Ordering Information

Device	Package	Shipping	
SSC8120GS6	SOT-23	3000/Reel	

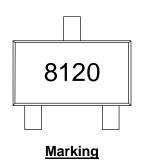
Pin configuration



SOT-23



Pin Configuration (Top View)





Absolute Maximum Ratings (T_A=25[°]C unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V _{DSS}	Drain-to-Source Voltage	20	V
V _{GSS}	Gate-to-Source Voltage	±12	V
I _D	Continuous Drain Current ^a	1.2	А
I _{DM}	Pulsed Drain Current b	3	А
P _D	Power Dissipation ^c	0.25	W
TJ	Operation junction temperature -55~150		$^{\circ}$ C
T _{STG}	Storage temperature range	-55~150	$^{\circ}\!\mathbb{C}$

➤ Thermal Resistance Ratings (T_A=25°C unless otherwise noted)

Symbol	Parameter	Maximum	Unit
Reja	Junction-to-Ambient Thermal Resistance a	499	°C/W
Rejc	Junction-to-Case Thermal Resistance	299	°C/W

Note:

- a. The value of R_{θJA} is measured with the device mounted on 1 in² FR-4 board with 2oz.copper, in a still air environment with T_A=25 °C. The value in any given application depends on the user is specific board design. The power dissipation is based on the t≤10s thermal resistance rating.
- b. Repetitive rating, pulse width limited by junction temperature.
- c. The power dissipation P_D is based on T_{J(MAX)}=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

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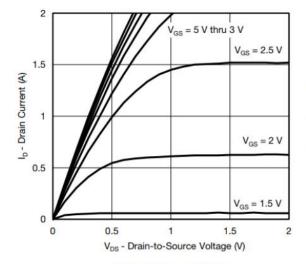


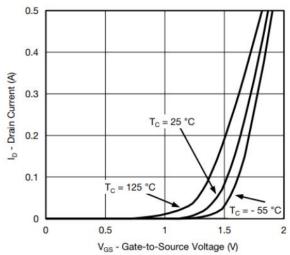
\succ Electrical Characteristics (T_A=25°C unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_{D} = 250\mu A$	20			V
Gate Threshold Voltage	$V_{\text{GS(th)}}$	$V_{DS} = V_{GS}$, $I_D = 250uA$	0.5	0.6	1	V
	R _{DS(on)}	$V_{GS} = 4.5V, I_D = 0.5A$		310	450	mΩ
Drain-Source On-Resistance		V _{GS} = 2.5V, I _D = 0.5A		490	765	
		V _{GS} = 1.8V, I _D = 0.35A		850	1300	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 16V, V _{GS} = 0V			1	μA
Gate-Source Leak Current	I _{GSS}	$V_{GS} = \pm 8V$, $V_{DS} = 0V$			±10	μA
Transconductance	G _{FS}	V _{DS} = 5V, I _D = 0.5A		11		S
Forward Voltage	V_{SD}	V _{GS} = 0V, I _S = 0.11A		0.7	1.3	V
Input Capacitance	Ciss	V 40V V 0V		110		
Output Capacitance	Coss	V _{DS} = 10V, V _{GS} = 0V,		15		pF
Reverse Transfer Capacitance	Crss	f = 1MHz		12		
Turn-on Delay Time	T _{D(ON)}	V _{GS} = 4.5V, I _D = 0.3A			5	
Turn-off Delay Time	T _{D(OFF)}	$V_{DS} = 5V$, $R_G = 3\Omega$			26	ns



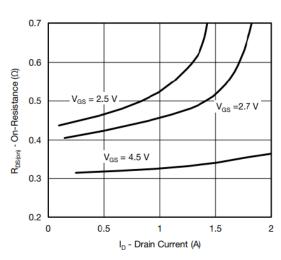
➤ Typical Performance Characteristics (T_A=25°C unless otherwise noted)

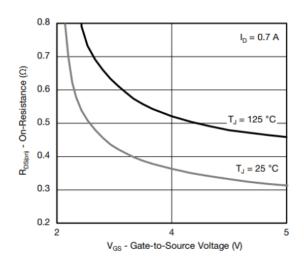




Output Characteristics

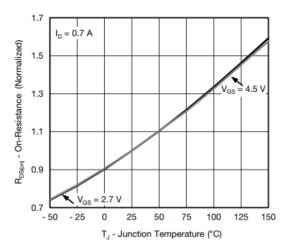
Transfer Characteristics





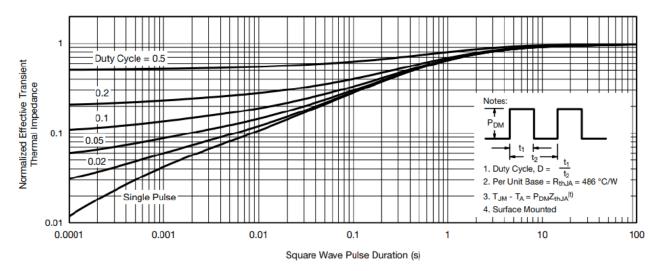
On-Resistance vs. Drain Current and Gate Voltage

On-Resistance vs. Gate-to-Source Voltage



On-Resistance vs. Junction Temperature

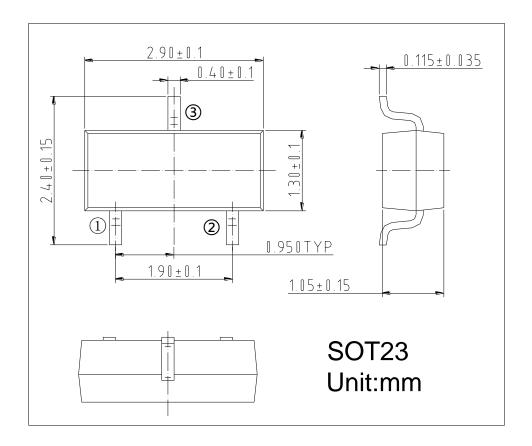




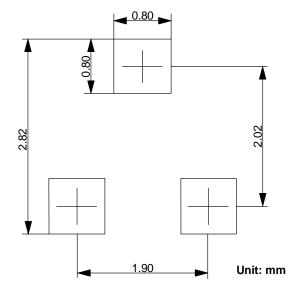
Normalized Thermal Transient Impedance, Junction-to-Ambient



Package Information



> Recommended Pad outline





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