



## SSC8322GN2

### Dual N-Channel Enhancement Mode MOSFET

#### ➤ Features

VDS	VGS	RDSON Typ.	ID
20V	±12V	40mR@4V5	4.4A
		50mR@2V5	

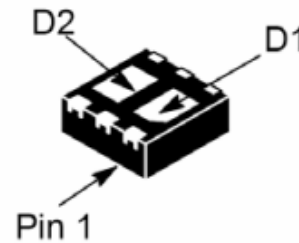
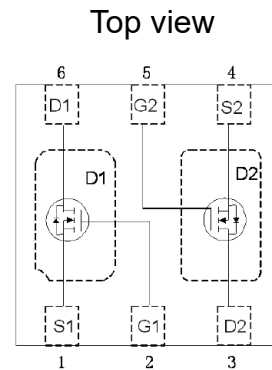
#### ➤ Description

SSC8322GN2 combines 2 N-Channel enhancement mode power MOSFETs which are produced with high cell density and DMOS trench technology. This device particularly suits low voltage applications, especially for battery powered circuits, the tiny and thin outline saves PCB consumption

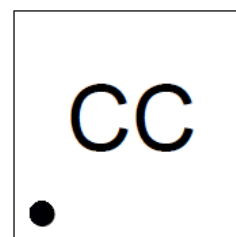
#### ➤ Applications

- Li Battery Charging
- High Side DC/DC Converter
- Load Switch
- Powered Devices
- Power Management in Portable, Battery

#### ➤ Pin configuration



Bottom View



Marking

#### ➤ Ordering Information

Device	Package	Shipping
SSC8322GN2	DFN2x2	3000/Reel



➤ **Absolute Maximum Ratings**( $T_A=25^{\circ}\text{C}$  unless otherwise noted)

Symbol	Parameter	Ratings	Unit
$V_{DSS}$	Drain-to-Source Voltage	20	V
$V_{GSS}$	Gate-to-Source Voltage	$\pm 12$	V
$I_D$	Continuous Drain Current <sup>a</sup>	4.4	A
$I_{DM}$	Pulsed Drain Current <sup>b</sup>	22	A
$P_D$	Power Dissipation <sup>c</sup>	2.2	W
$P_{DSM}$	Power Dissipation <sup>a</sup>	1.1	W
$T_J$	Operation junction temperature	-55 to 150	$^{\circ}\text{C}$
$T_{STG}$	Storage temperature range	-55 to 150	$^{\circ}\text{C}$

➤ **Thermal Resistance Ratings**( $T_A=25^{\circ}\text{C}$  unless otherwise noted)

Symbol	Parameter	Typical	Maximum	Unit
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance <sup>a</sup>		120	$^{\circ}\text{C}/\text{W}$
$R_{\theta JC}$	Junction-to-Case Thermal Resistance		60	

Note:

- The value of  $R_{\theta JA}$  is measured with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz.copper,in a still air environment with  $T_A=25^{\circ}\text{C}$ .The value in any given application depends on the user is specific board design. The current rating is based on the  $t \leq 10\text{s}$  thermal resistance rating.
- Repetitive rating, pulse width limited by junction temperature.
- The power dissipation  $P_D$  is based on  $T_J(\text{MAX})=150^{\circ}\text{C}$ , using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

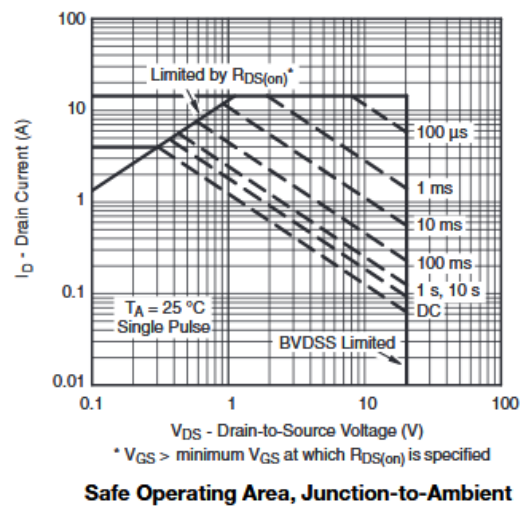
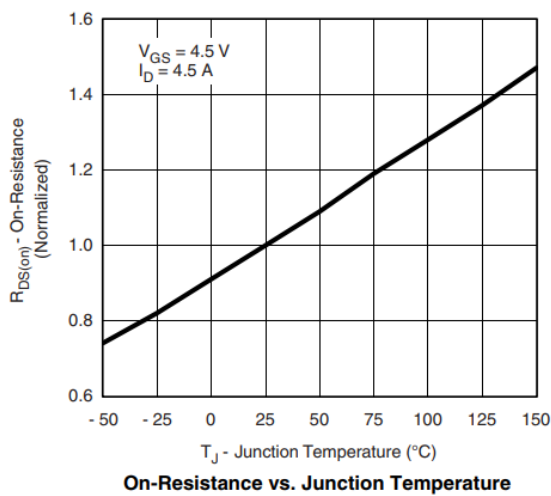
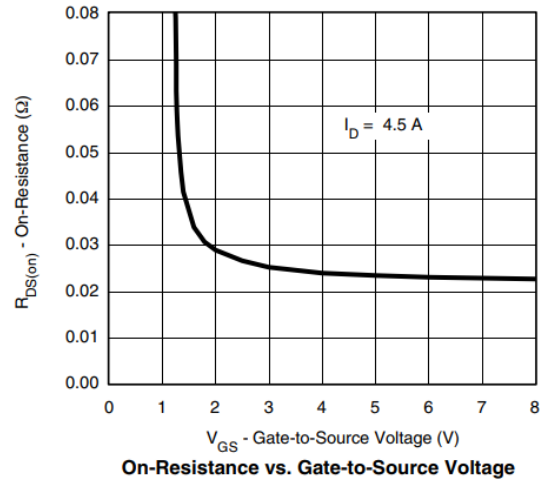
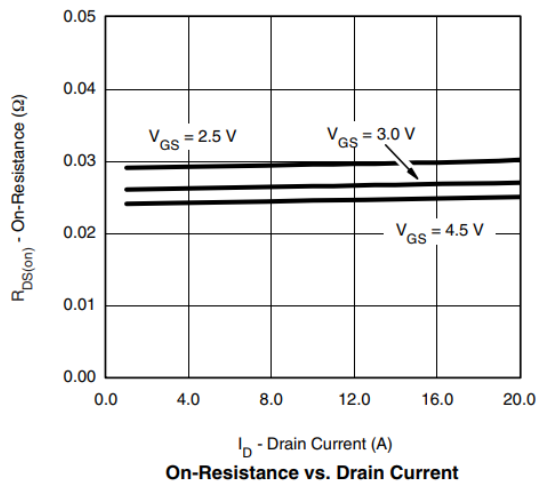
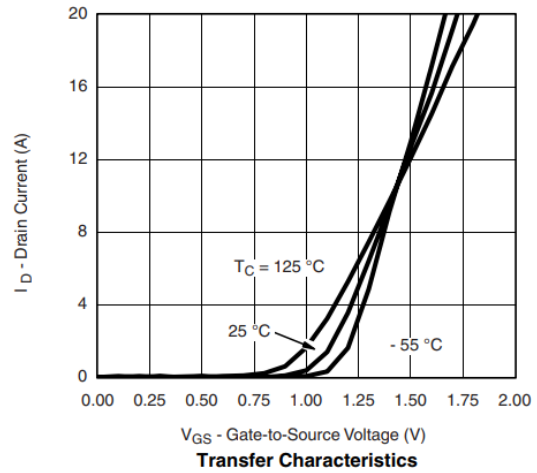
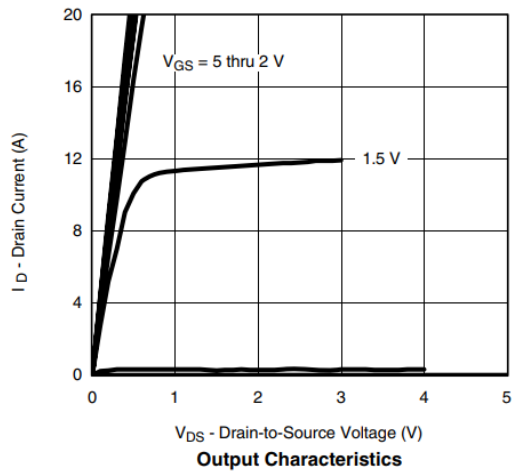


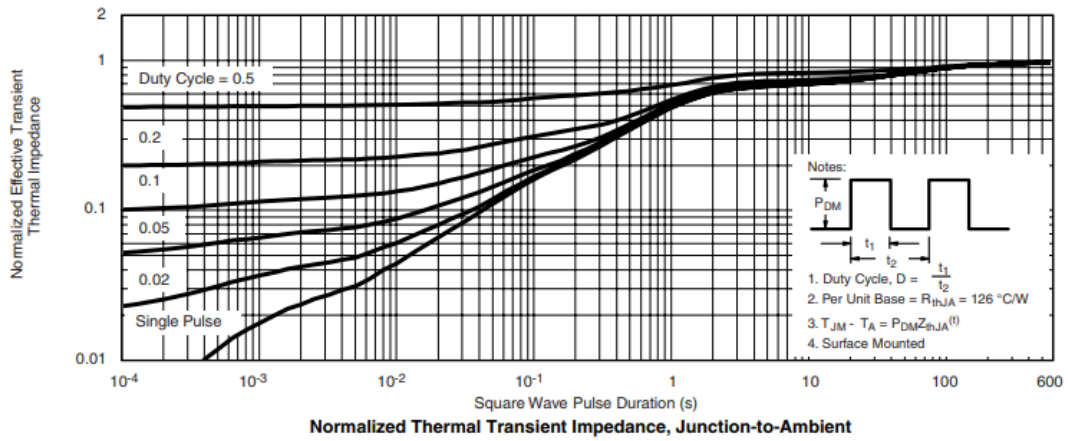
➤ **Electronics Characteristics**( $T_A=25^{\circ}\text{C}$  unless otherwise noted)

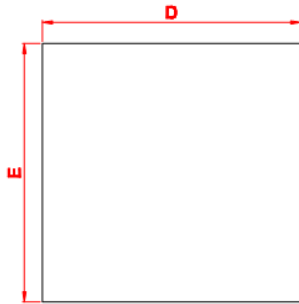
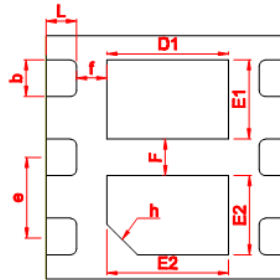
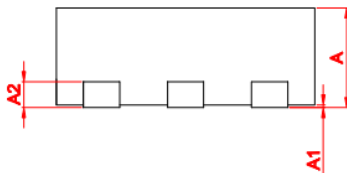
Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	20			V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	0.4	0.7	1.2	V
$R_{DS(on)}$	Drain-Source On- Resistance	$V_{GS}=4.5V, I_D=3.6A$		40	60	mR
		$V_{GS}=2.5V, I_D=3.1A$		50	80	
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=20V, V_{GS}=0V$			1	$\mu A$
$I_{GSS}$	Gate-Source leak current	$V_{GS}=\pm 12V, V_{DS}=0V$			$\pm 100$	nA
$V_{SD}$	Forward Voltage	$V_{GS}=0V, I_S=1.1A$		0.8	1.15	V
$G_{FS}$	Transconductance	$V_{DS}=5V, I_D=3.6A$		13		S
$C_{iss}$	Input Capacitance	$V_{DS}=10V, V_{GS}=0V, f=1MHz$		450		pF
$C_{oss}$	Output Capacitance			70		
$C_{rss}$	Reverse Transfer Capacitance			43		
$Q_g$	Total Gate charge	$V_{GS}=4.5V, V_{DS}=15V, I_D=3A$		3		nC
$Q_{gs}$	Gate to Source charge			0.6		
$Q_{gd}$	Gate to Drain charge			1.1		
$T_{D(ON)}$	Turn-on delay time	$V_{GS}=4.5V, V_{DS}=5V, R_G=6R, I_D=3.6A$		15		ns
$T_r$	Rise time			18		
$T_{D(OFF)}$	Turn-off delay time			60		
$T_f$	Fall time			20		



➤ Typical Characteristics ( $T_A=25^\circ\text{C}$  unless otherwise noted)





**➤ Package Information**

**TOP VIEW**

**BOTTOM VIEW**

**SIDE VIEW**

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.700	0.750	0.800
* A1	0.000	0.020	0.050
* b	0.275	0.300	0.325
* A2	0.190	0.210	0.230
* D	1.900	2.000	2.100
* E	1.900	2.000	2.100
* E1	0.570	0.620	0.670
* E2	0.570	0.620	0.670
* D1	0.950	1.000	1.050
* D2	0.950	1.000	1.050
* e	0.800	0.850	0.700
h	0.300	0.350	0.400
* L	0.200	0.250	0.300
* F	0.250	0.300	0.350
* f	0.200	0.260	0.300

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