

SSC8122GN1

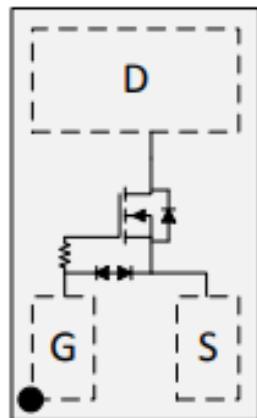
N-Channel Enhancement Mode MOSFET with ESD protection

➤ Features

VDS	VGS	RDS(on) Typ.	ID	ESD
20V	±8V	195mR@4V5	1.1A	2K
		240mR@2V5		
		305mR@1V8		

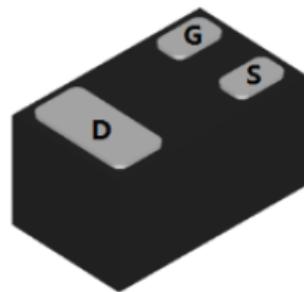
➤ Pin configuration

Top view



➤ Description

This device is a N-Channel enhancement mode MOSFET which is produced with high cell density and DMOS trench technology. This device particularly suits low voltage applications, especially for battery powered circuits, the tiny and thin outline saves PCB consumption.



Bottom View



Marking

➤ Ordering Information

Device	Package	Shipping
SSC8122GN1	DFN1006	10K/Reel

➤ **Absolute Maximum Ratings($T_A=25^\circ\text{C}$ unless otherwise noted)**

Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain-to-Source Voltage	20	V
V_{GSS}	Gate-to-Source Voltage	± 8	V
I_D	Continuous Drain Current ^a	1.1	A
I_{DM}	Pulsed Drain Current ^b	3.1	A
P_D	Power Dissipation ^c	0.32	W
P_{DSM}	Power Dissipation ^a	0.18	W
T_J	Operation junction temperature	-55 to 150	$^\circ\text{C}$
T_{STG}	Storage temperature range	-55 to 150	$^\circ\text{C}$

➤ **Thermal Resistance Ratings($T_A=25^\circ\text{C}$ unless otherwise noted)**

Symbol	Parameter	Typical	Maximum	Unit
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance ^a		690	$^\circ\text{C}/\text{W}$
$R_{\theta JC}$	Junction-to-Case Thermal Resistance		379	

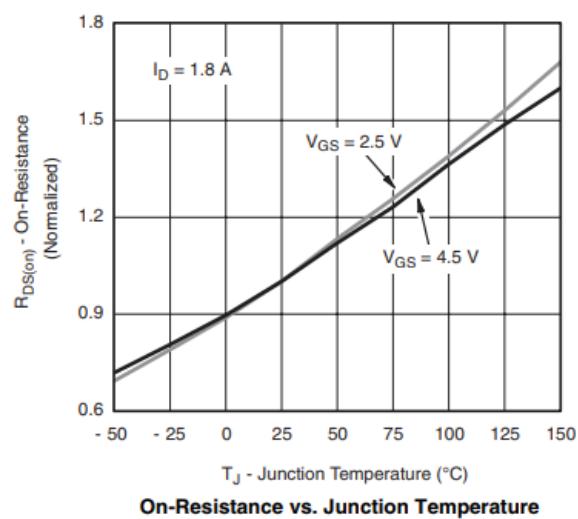
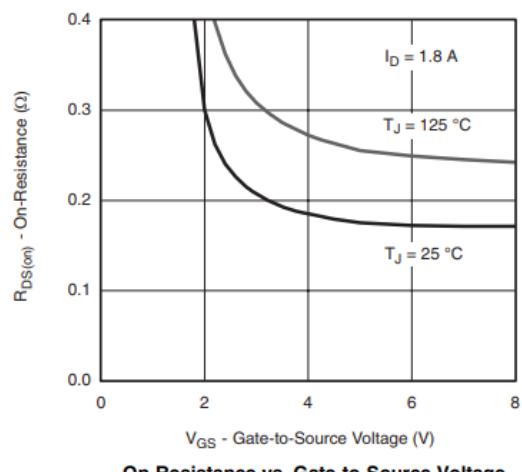
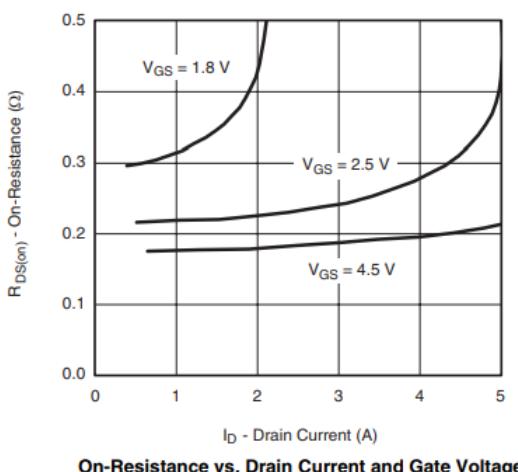
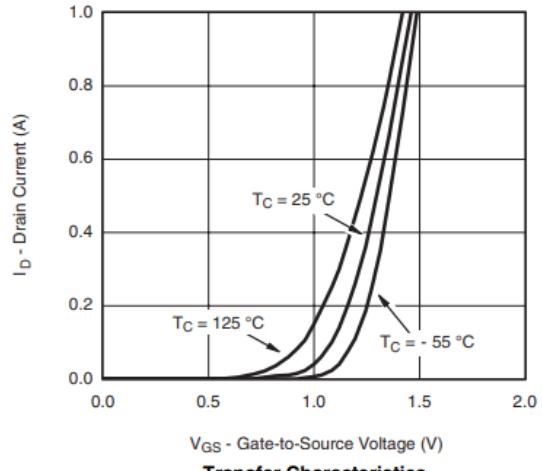
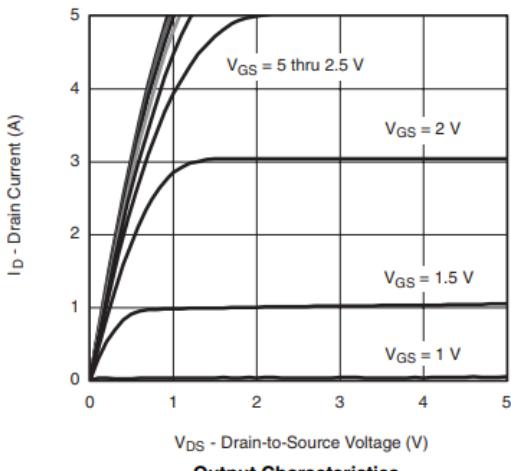
Note:

- a. The value of $R_{\theta JA}$ is measured with the device mounted on 1 in² FR-4 board with 2oz.copper,in a still air environment with $T_A=25^\circ\text{C}$.The value in any given application depends on the user specific board design. The current rating is based on the $t \leq 10\text{s}$ thermal resistance rating.
- b. Repetitive rating, pulse width limited by junction temperature.
- c. The power dissipation P_D is based on $T_{J(MAX)}=150^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

➤ Electronics Characteristics($T_A=25^\circ C$ unless otherwise noted)

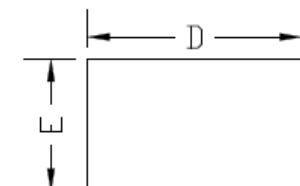
Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$VGS=0V$, $ID=250\mu A$	20			V
$V_{GS(th)}$	Gate Threshold Voltage	$VDS=VGS$, $ID=250\mu A$	0.5	0.68	1	V
$R_{DS(on)}$	Drain-Source On-Resistance	$VGS=4.5V$, $ID=0.5A$		195	310	mR
		$VGS=2.5V$, $ID=0.5A$		240	380	
		$VGS=1.8V$, $ID=0.35A$		305	450	
I_{DSS}	Zero Gate Voltage Drain Current	$VDS=20V$, $VGS=0V$			1	μA
I_{GSS}	Gate-Source leak current	$VGS=\pm 8V$, $VDS=0V$			± 10	μA
G_{FS}	Transconductance	$VDS=5V$, $ID=0.5A$		2		S
V_{SD}	Forward Voltage	$VGS=0V$, $IS=0.5A$		0.7	1.3	V
C_{iss}	Input Capacitance	$VDS=10V$, $VGS=0V$, $f=1MHz$		66		pF
C_{oss}	Output Capacitance			18		
C_{rss}	Reverse Transfer Capacitance			9		
$T_{D(ON)}$	Turn-on delay time	$VGS=4.5V$, $VDS=10V$, $RG=6R$, $ID=0.6A$		20		ns
Tr	Rise time			13		
$T_{D(OFF)}$	Turn-off delay time			40		
Tf	Fall time			12		

➤ **Typical Characteristics**($T_A=25^\circ\text{C}$ unless otherwise noted)

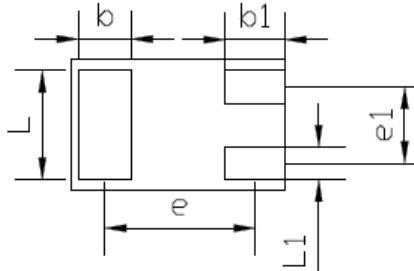


➤ Package Information

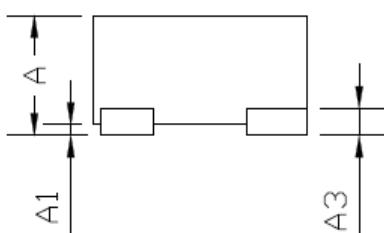
POD



TOP VIEW



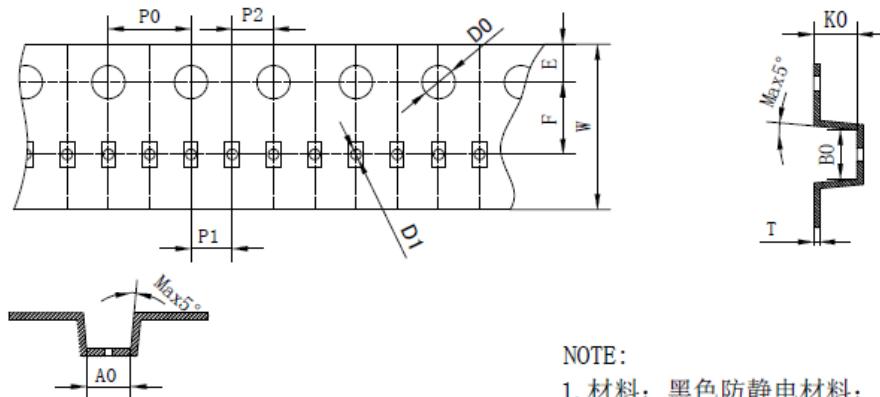
BOTTOM VIEW



SIDE VIEW

COMMON DIMENSION (MM)			
PKG	DFN1006		
REF.	MIN.	NOM.	MAX
A	>0.4	-	0.50
A1	0.00	-	0.05
A3	0.125REF.		
D	0.95	1.00	1.05
E	0.55	0.60	0.65
b	0.20	0.25	0.30
b1	0.20	0.30	0.40
L	0.45	0.50	0.55
L1	0.10	0.15	0.20
e	0.675		
e1	0.35		

Tape Data

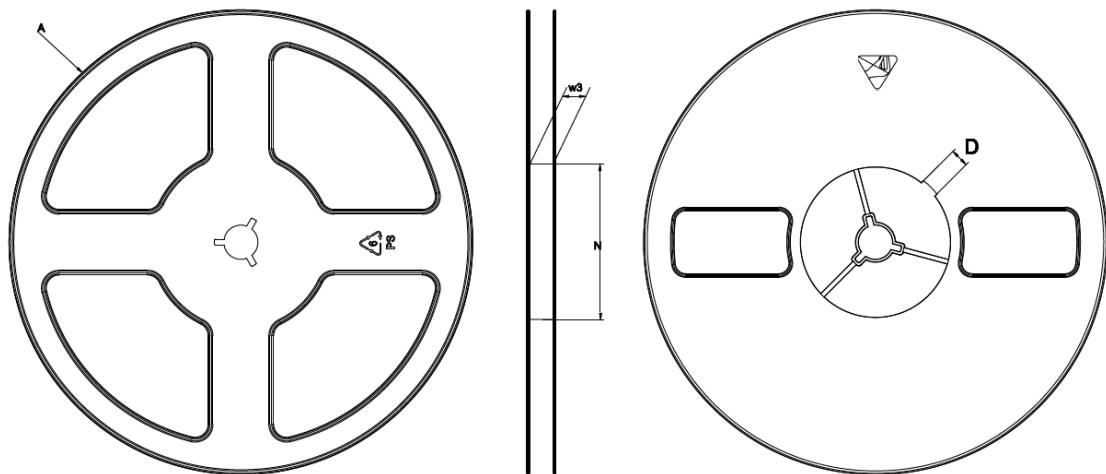


NOTE:

1. 材料: 黑色防静电材料;
2. 10个链孔的累积公差不能超过±0.2
3. 尺寸符合EIA-481-E的要求。

SYMBOL	A0	B0	K0	P0	P1	P2
SPEC	0.69 ± 0.05	1.15 ± 0.05	0.60 ± 0.05	4.00 ± 0.10	2.00 ± 0.05	2.00 ± 0.05
SYMBOL	T	E	F	D0	D1	W
SPEC	0.18 ± 0.03	1.75 ± 0.10	3.50 ± 0.05	1.55 ± 0.05	0.50 ± 0.05	$8.00^{+0.5}_{-0.1}$

Reel Data



材质说明：该产品用料为 PS

TYPE	A	N	C	D	w3
8MM	$\varnothing 178^{+1}_{-1}$	$\varnothing 60^{-1}$	$\varnothing 13,3^{-0,3}$	$7,5 \pm 0,5$	$9 \pm 0,3$

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