SSC8124GS6

N-Channel Enhancement Mode MOSFET

➢ Features

VDS	VGS	RDSON Typ.	ID
20V	±12V	23mR@4V5	5.5A
		29mR@2V5	
		47mR@1V8	

➢ Description

This device is a N-Channel enhancement mode MOSFET which is produced with high cell density and DMOS trench technology. This device particularly suits low voltage applications, especially for battery powered circuits, the tiny and thin outline saves PCB consumption.

➢ Applications

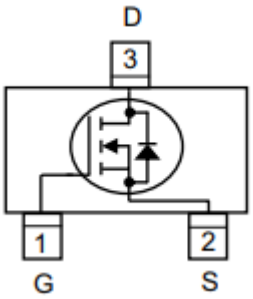
- Load Switch
- Portable Devices
- DCDC conversion

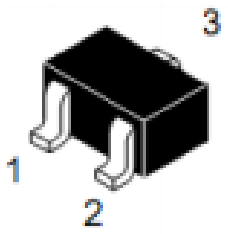
➢ Ordering Information

Device	Package	Shipping
SSC8124GS6	SOT23	3000/Reel

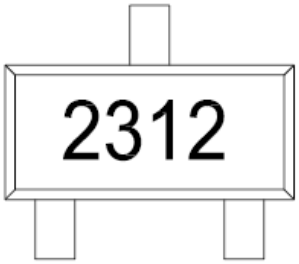
➢ Pin configuration

Top view





SOT-23



Marking

➢ Absolute Maximum Ratings(T_A=25℃ unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain-to-Source Voltage	20	V
V_{GSS}	Gate-to-Source Voltage	±12	V
I_D	Continuous Drain Current [a]	5.5	A
I_{DM}	Pulsed Drain Current [b]	15	A
P_D	Power Dissipation [c]	1	W
P_{DSM}	Power Dissipation [a]	0.55	W
T_J	Operation junction temperature	-55 to 150	℃
T_{STG}	Storage temperature range	-55 to 150	℃

➢ Thermal Resistance Ratings(T_A=25℃ unless otherwise noted)

Symbol	Parameter	Typical	Maximum	Unit
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance [a]		240	℃/W
$R_{\theta JC}$	Junction-to-Case Thermal Resistance		130	

Note:

a. The value of $R_{\theta JA}$ is measured with the device mounted on 1 in^2 FR-4 board with 2oz.copper,in a still air environment with T_A=25℃.The value in any given application depends on the user is specific board design. The current rating is based on the t≤ 10s thermal resistance rating.

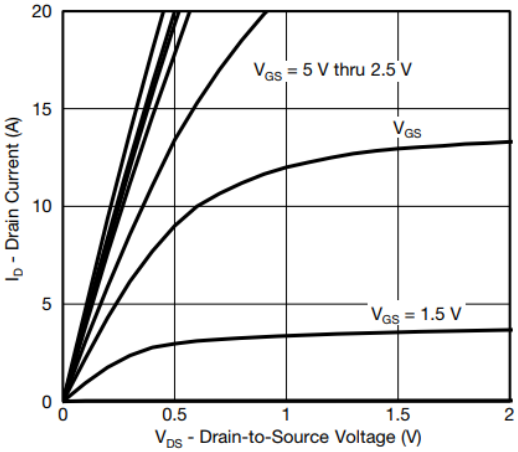
b. Repetitive rating, pulse width limited by junction temperature.

c. The power dissipation P_D is based on $T_{J(MAX)}$=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

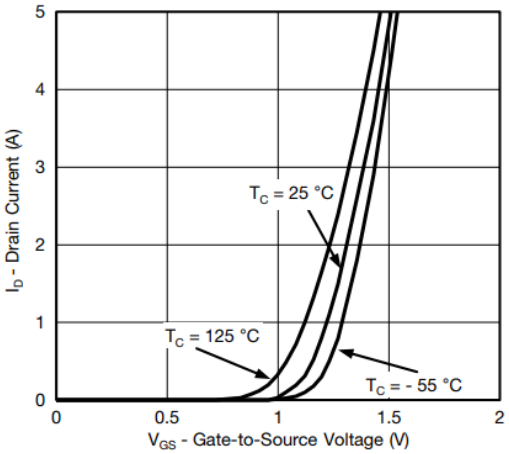
➢ **Electronics Characteristics**(T_A=25℃ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	VGS=0V,ID=250uA	20			V
$V_{GS\ (th)}$	Gate Threshold Voltage	VDS=VGS,ID=250uA	0.4	0.78	0.9	V
$R_{DS(on)}$	Drain-Source On-Resistance	VGS=4.5V,ID=5A		23	27	mR
		VGS=2.5V,ID=3.5A		29	34	
		VGS=1.8V,ID=2.8A		47	55	
I_{DSS}	Zero Gate Voltage Drain Current	VDS=20V,VGS=0V			1	uA
I_{GSS}	Gate-Source leak current	VGS=±12V,VDS=0V			±100	nA
G_{FS}	Transconductance	VDS=5V,ID=3.6A		7	14	S
V_{SD}	Forward Voltage	VGS=0V,IS=1.1A		0.8	1.2	V
Ciss	Input Capacitance	VDS=10V, VGS=0V, f=1MHz		460		pF
Coss	Output Capacitance			80		
Crss	Reverse Transfer Capacitance			46		
$T_{D(ON)}$	Turn-on delay time	VGS=4.5V, VDS=5V, RG=6R,ID=3.6A		15		ns
Tr	Rise Time			11		
$T_{D(OFF)}$	Turn-off delay time			60		
Tf	Fall Time			20		
Qg	Total Gate charge	VGS=4.5V, VDS=10V, ID=4A		11		nC
Qgs	Gate to Source charge			1.1		
Qgd	Gate to Drain charge			3.3		

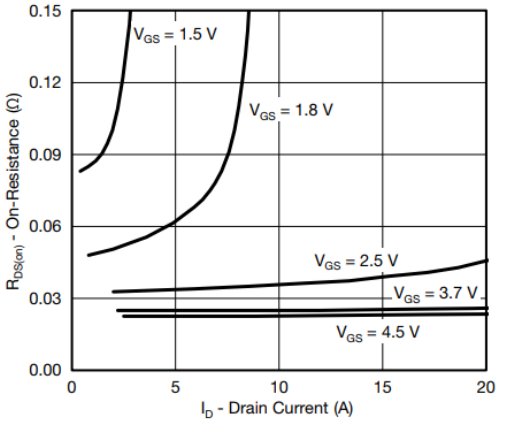
➢ Typical Characteristics(T_A=25℃ unless otherwise noted)



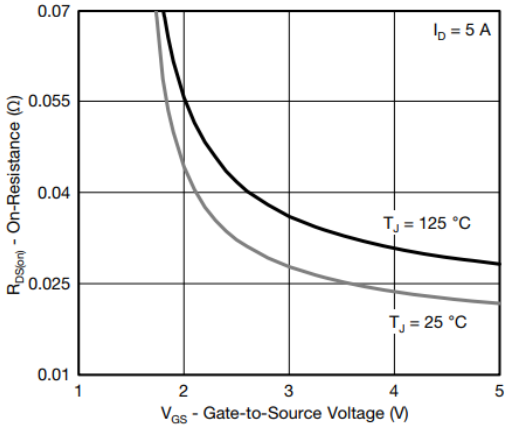
Output Characteristics



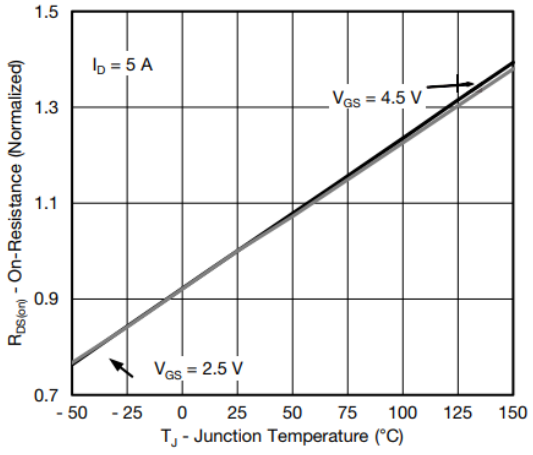
Transfer Characteristics



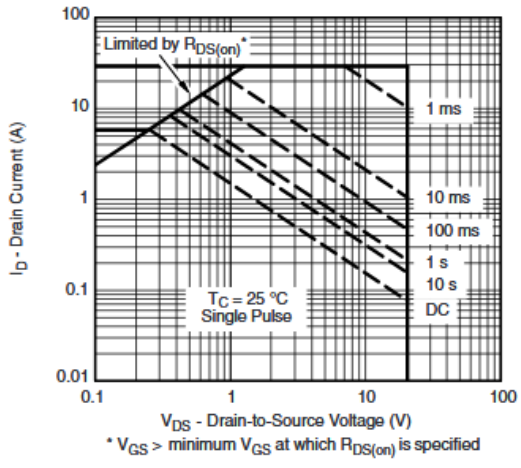
On-Resistance vs. Drain Current and Gate Voltage



On-Resistance vs. Gate-to-Source Voltage

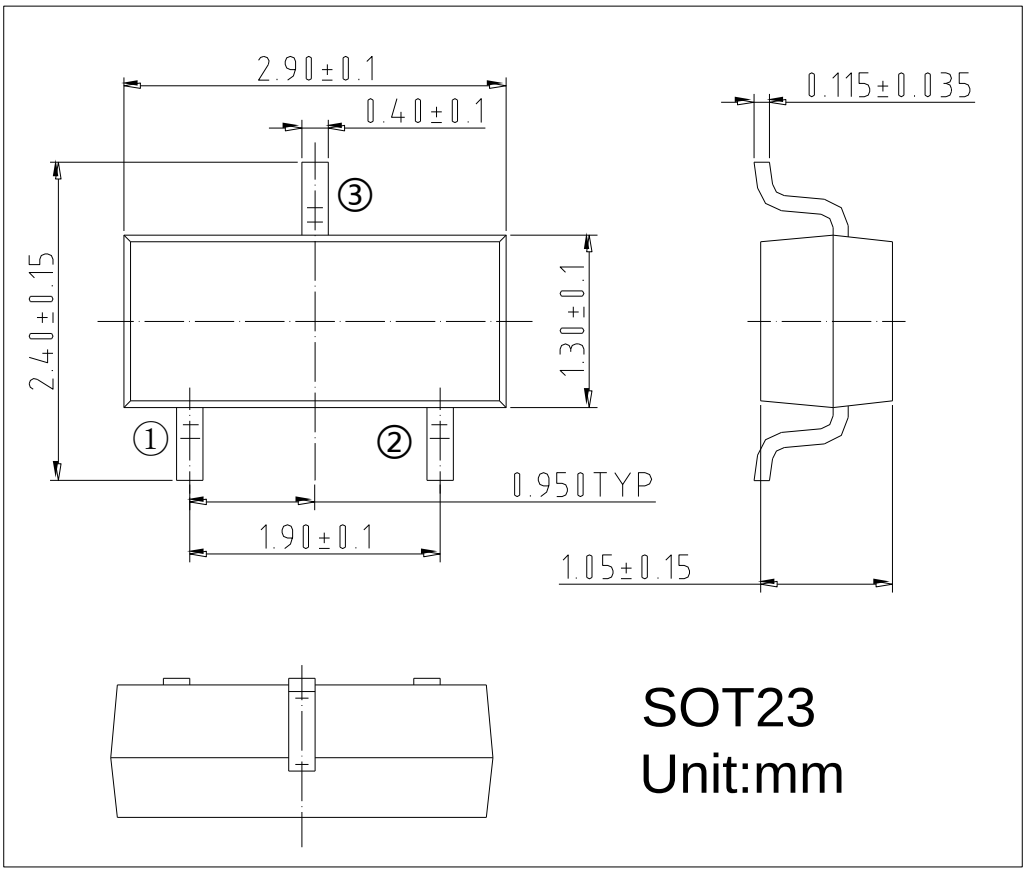


On-Resistance vs. Junction Temperature



Safe Operating Area, Junction-to-Case

➢ Package Information



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