



## SSC8164GS6

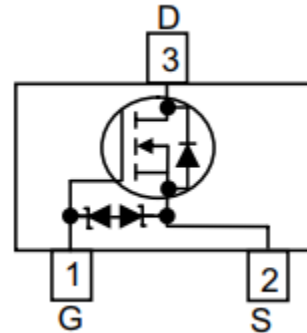
### N-Channel Small Switching MOSFET with ESD Protection

#### ➤ Features

VDS	VGS	RDS(on) Typ.	ID	ESD
60V	±20V	1.1R@10V	0.5A	500V
		1.5R@4V5		

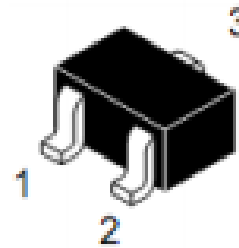
#### ➤ Pin configuration

Top view



#### ➤ Description

This device is an N-Channel enhancement mode MOSFET which is produced with high cell density and DMOS trench technology. This device particularly suits low voltage applications, especially for battery powered circuits, the tiny and thin outline saves PCB consumption.



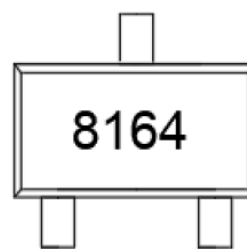
SOT23

#### ➤ Applications

- Load Switch
- Portable Devices
- DCDC Conversion

#### ➤ Ordering Information

Device	Package	Shipping
SSC8164GS6	SOT23	3000/Reel



Marking



➤ **Absolute Maximum Ratings**( $T_A=25^{\circ}\text{C}$  unless otherwise noted)

Symbol	Parameter	Ratings	Unit
$V_{DSS}$	Drain-to-Source Voltage	60	V
$V_{GSS}$	Gate-to-Source Voltage	$\pm 20$	V
$I_D$	Continuous Drain Current <sup>a</sup>	0.5	A
$I_{DM}$	Pulsed Drain Current <sup>b</sup>	1	A
$P_D$	Power Dissipation <sup>c</sup>	0.85	W
$P_{DSM}$	Power Dissipation <sup>a</sup>	0.36	W
$T_J$	Operation junction temperature	-55 to 150	$^{\circ}\text{C}$
$T_{STG}$	Storage temperature range	-55 to 150	$^{\circ}\text{C}$

➤ **Thermal Resistance Ratings**( $T_A=25^{\circ}\text{C}$  unless otherwise noted)

Symbol	Parameter	Typical	Maximum	Unit
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance <sup>a</sup>		360	$^{\circ}\text{C}/\text{W}$
$R_{\theta JC}$	Junction-to-Case Thermal Resistance		155	

Note:

- The value of  $R_{\theta JA}$  is measured with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz.copper, in a still air environment with  $T_A=25^{\circ}\text{C}$ . The value in any given application depends on the user is specific board design. The current rating is based on the  $t \leq 10\text{s}$  thermal resistance rating.
- Repetitive rating, pulse width limited by junction temperature.
- The power dissipation  $P_D$  is based on  $T_{J(MAX)}=150^{\circ}\text{C}$ , using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

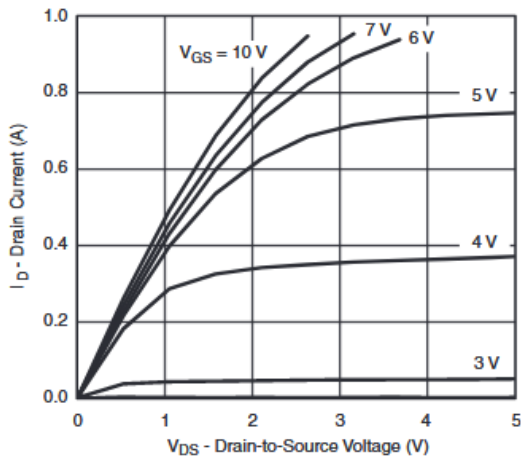


➤ **Electronics Characteristics**( $T_A=25^{\circ}\text{C}$  unless otherwise noted)

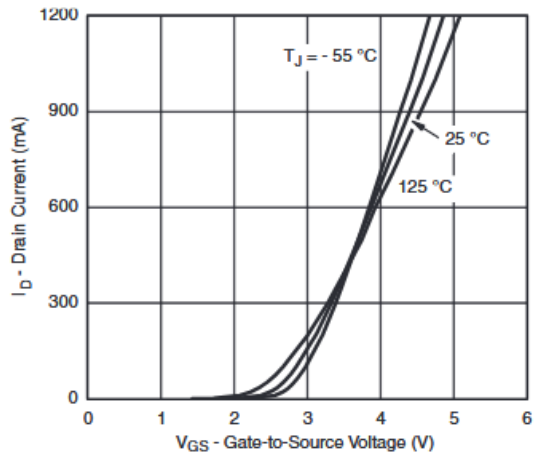
Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=10\mu A$	60			V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	0.75	1	1.25	V
$R_{DS(on)}$	Drain-Source On- Resistance	$V_{GS}=10V, I_D=0.5A$		1.1	2.5	R
		$V_{GS}=4.5V, I_D=0.5A$		1.5	3.5	
		$V_{GS}=2.5V, I_D=0.5A$		1.7	4	
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=60V, V_{GS}=0V$			1	$\mu A$
$I_{GSS}$	Gate-Source leak current	$V_{GS}=\pm 15V, V_{DS}=0V$			$\pm 10$	$\mu A$
$G_{FS}$	Transconductance	$V_{DS}=10V, I_D=0.2A$		0.1		S
$V_{SD}$	Forward Voltage	$V_{GS}=0V, I_S=0.2A$			1.3	V
$C_{iss}$	Input Capacitance	$V_{DS}=25V, V_{GS}=0V, f=1MHz$		30		pF
$C_{oss}$	Output Capacitance			6		
$C_{rss}$	Reverse Transfer Capacitance			2.9		
$T_{D(ON)}$	Turn-on delay time			25		
$T_r$	Rise Time	$V_{GS}=10V,$ $V_{DS}=10V, I_D=100mA$		10		ns
$T_{D(OFF)}$	Turn-off delay time			35		
$T_f$	Fall Time			20		
$Q_G$	Total Gate Charge			0.4		
$Q_{GS}$	Gate Source Charge	$V_{GS}=10V, V_{DS}=15V, I_D=0.2A$		0.1		nC
$Q_{GD}$	Gate Drain Charge			0.11		



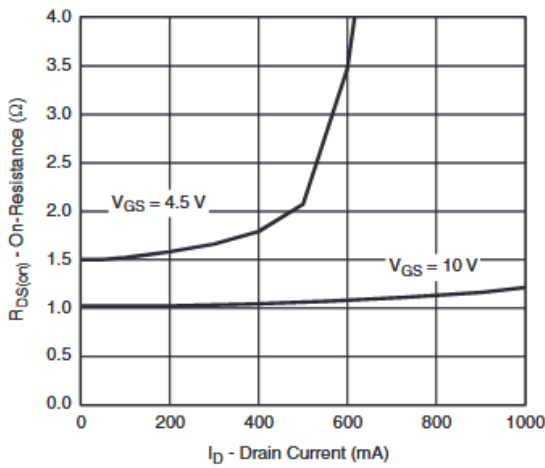
➤ **Typical Characteristics** ( $T_A=25^\circ\text{C}$  unless otherwise noted)



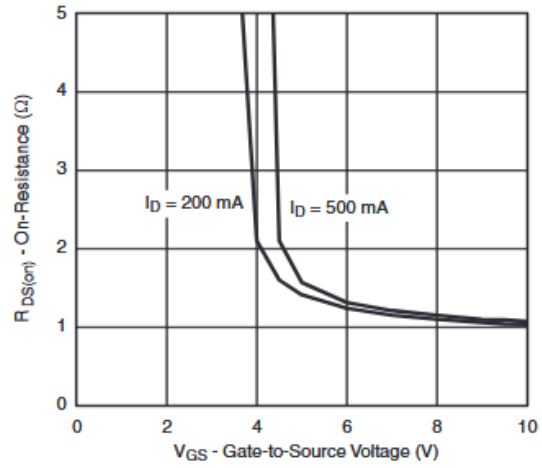
**Output Characteristics**



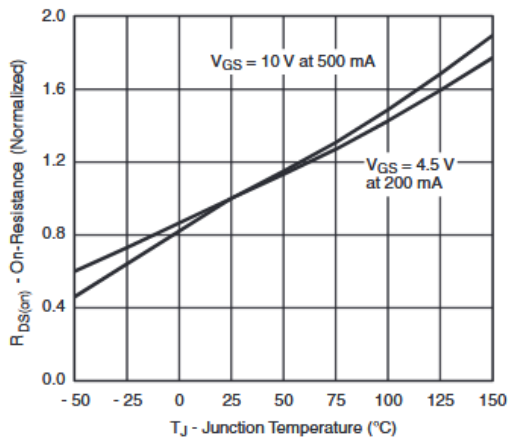
**Transfer Characteristics**



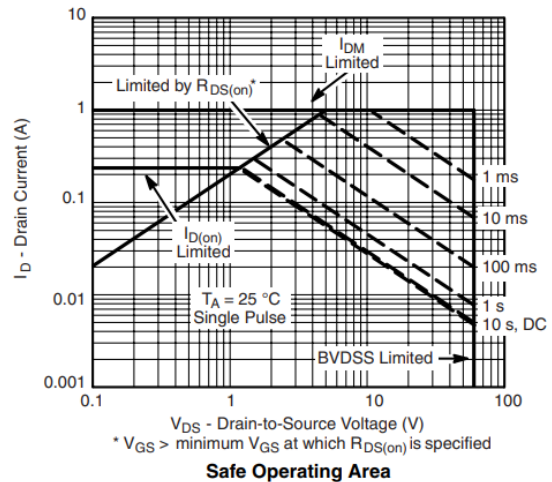
**On-Resistance vs. Drain Current**



**On-Resistance vs. Gate-Source Voltage**



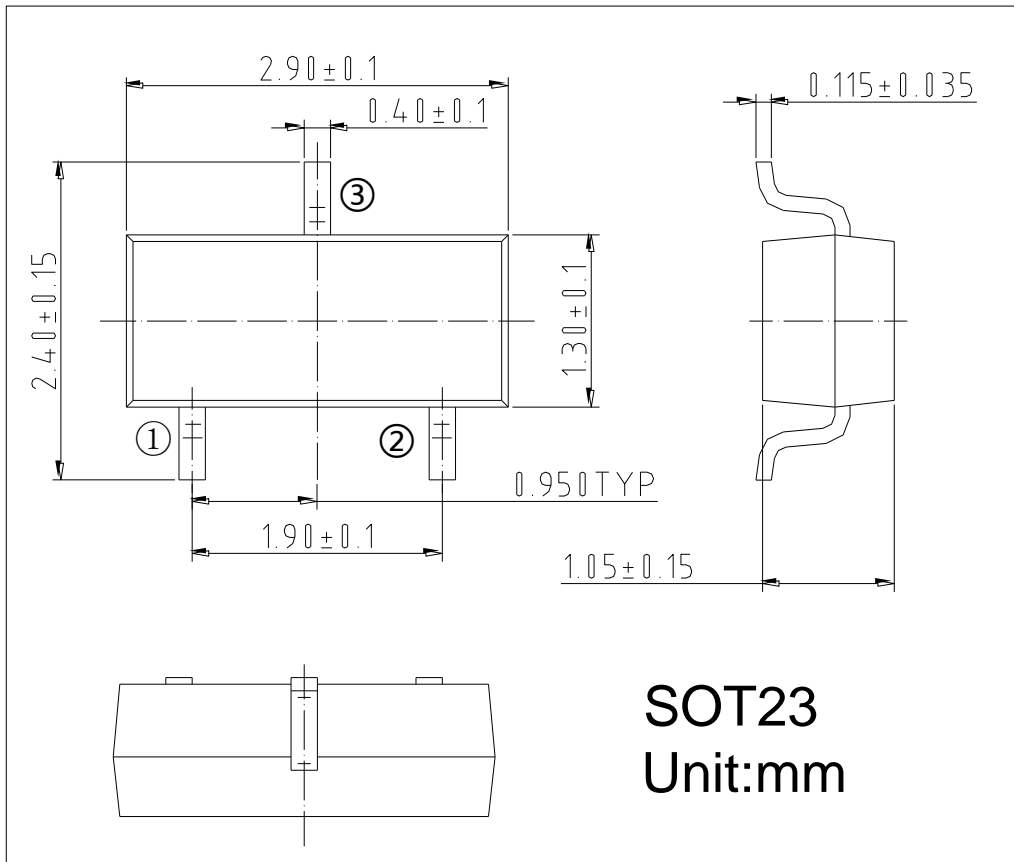
**On-Resistance vs. Junction Temperature**



**Safe Operating Area**



➤ Package Information



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