



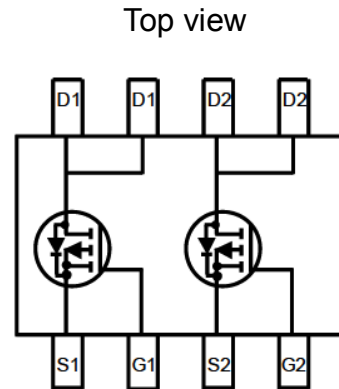
# SSC8329GS1

## Dual P-Channel Enhancement Mode MOSFET

### ➤ Features

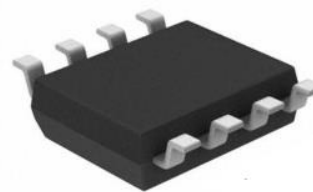
VDS	VGS	RDSON Typ.	ID
-20V	±12V	13mR@-4V5	-13A
		16mR@-2V5	

### ➤ Pin configuration



### ➤ Description

This device is produced with high cell density, DMOS trench technology, which is especially used to minimize on-state resistance. This device is particularly suited for low voltage power management requiring a wide range of given voltage ratings(4.5V~25V) such as load switch and battery protection.



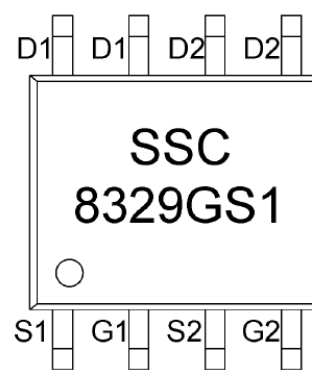
Bottom View

### ➤ Applications

- NB Battery
- DC/DC Conversion
- Load Switch

### ➤ Ordering Information

Device	Package	Shipping
SSC8329GS1	SOP-8	2500/Reel



Marking



➤ **Absolute Maximum Ratings**( $T_A=25^{\circ}\text{C}$  unless otherwise noted)

Symbol	Parameter	Ratings	Unit
$V_{DSS}$	Drain-to-Source Voltage	-20	V
$V_{GSS}$	Gate-to-Source Voltage	$\pm 12$	V
$I_D$	Continuous Drain Current <sup>a</sup>	-13	A
$I_{DM}$	Pulsed Drain Current <sup>b</sup>	-51	A
$P_D$	Power Dissipation <sup>c</sup>	5.4	W
$P_{DSM}$	Power Dissipation <sup>a</sup>	2.2	W
$T_J$	Operation junction temperature	-55 to 150	$^{\circ}\text{C}$
$T_{STG}$	Storage temperature range	-55 to 150	$^{\circ}\text{C}$

➤ **Thermal Resistance Ratings**( $T_A=25^{\circ}\text{C}$  unless otherwise noted)

Symbol	Parameter	Typical	Maximum	Unit
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance <sup>a</sup>		60	$^{\circ}\text{C}/\text{W}$
$R_{\theta JC}$	Junction-to-Case Thermal Resistance		25	

Note:

- The value of  $R_{\theta JA}$  is measured with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz.copper,in a still air environment with  $T_A=25^{\circ}\text{C}$ .The value in any given application depends on the user is specific board design. The current rating is based on the  $t \leq 10\text{s}$  thermal resistance rating.
- Repetitive rating, pulse width limited by junction temperature.
- The power dissipation  $P_D$  is based on  $T_J(\text{MAX})=150^{\circ}\text{C}$ , using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

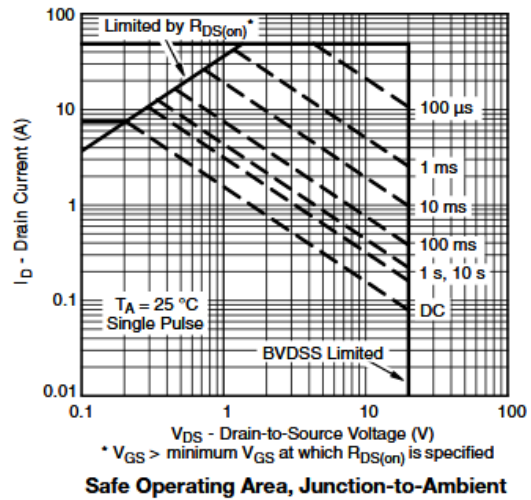
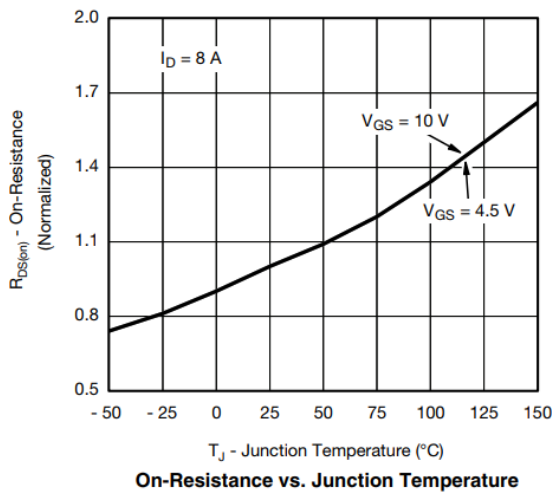
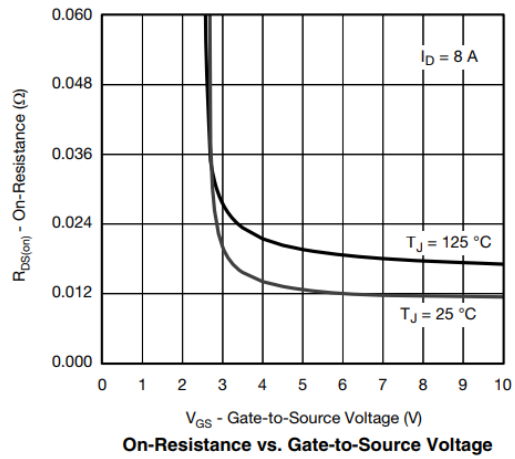
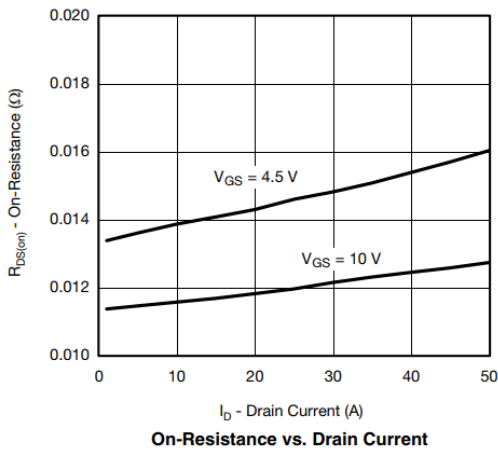
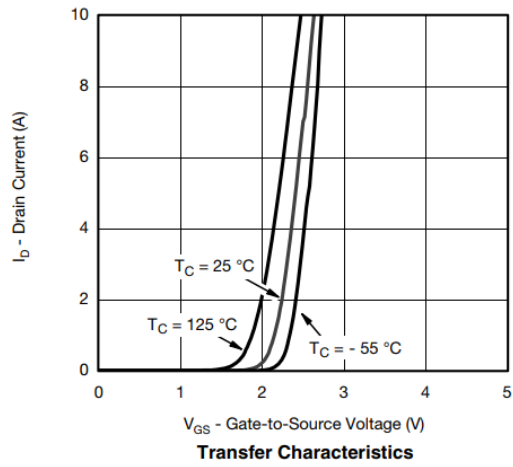
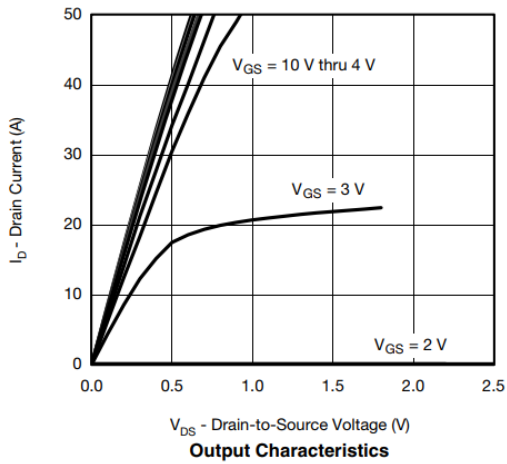


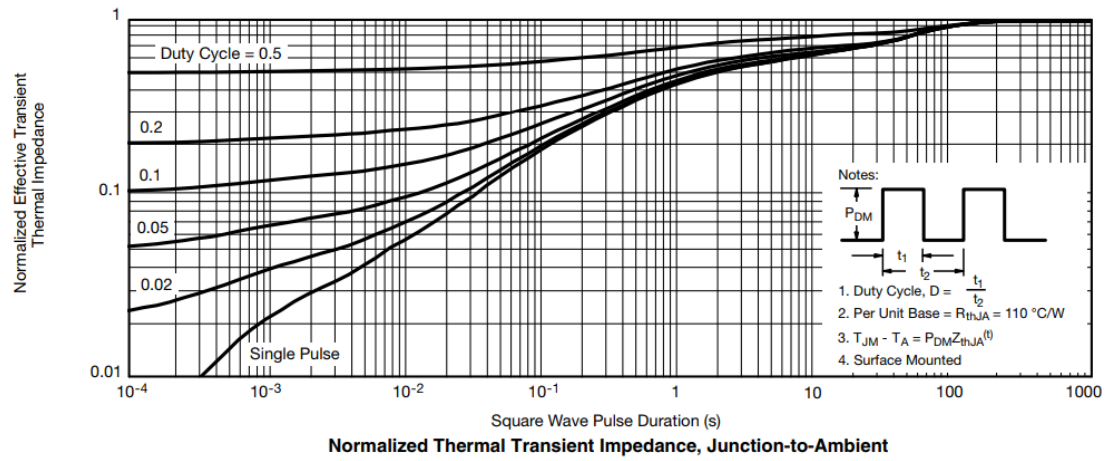
➤ **Electronics Characteristics**( $T_A=25^{\circ}\text{C}$  unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-20			V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=-250\mu A$	-0.5		-1	V
$R_{DS(on)}$	Drain-Source On- Resistance	$V_{GS}=-4.5V, I_D=-10A$		13	15	mR
		$V_{GS}=-2.5V, I_D=-7A$		16	18	
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=-16V, V_{GS}=0V$			-1	$\mu A$
$I_{GSS}$	Gate-Source leak current	$V_{GS}=\pm 12V, V_{DS}=0V$			$\pm 100$	nA
$V_{SD}$	Forward Voltage	$V_{GS}=0V, I_S=-2.3A$		-0.7	-1.3	V
$G_{FS}$	Transconductance	$V_{DS}=-10V, I_D=-3.6A$		16		S
$C_{iss}$	Input Capacitance	$V_{DS}=-15V, V_{GS}=0V, f=1MHz$		1020		pF
$C_{oss}$	Output Capacitance			110		
$C_{rss}$	Reverse Transfer Capacitance			90		
$T_{D(ON)}$	Turn-on delay time			11		
$T_r$	Rise time	$V_{GS}=-10V,$ $V_{DS}=-15V, R_G=3R, R_L=1.5R$		10		ns
$T_{D(OFF)}$	Turn-off delay time			51		
$T_f$	Fall time			29		
$Q_g$	Total Gate charge			13		
$Q_{gs}$	Gate to Source charge	$V_{GS}=-4.5V, V_{DS}=-15V,$ $I_D=-3A$		3.3		nC
$Q_{gd}$	Gate to Drain charge			4.4		



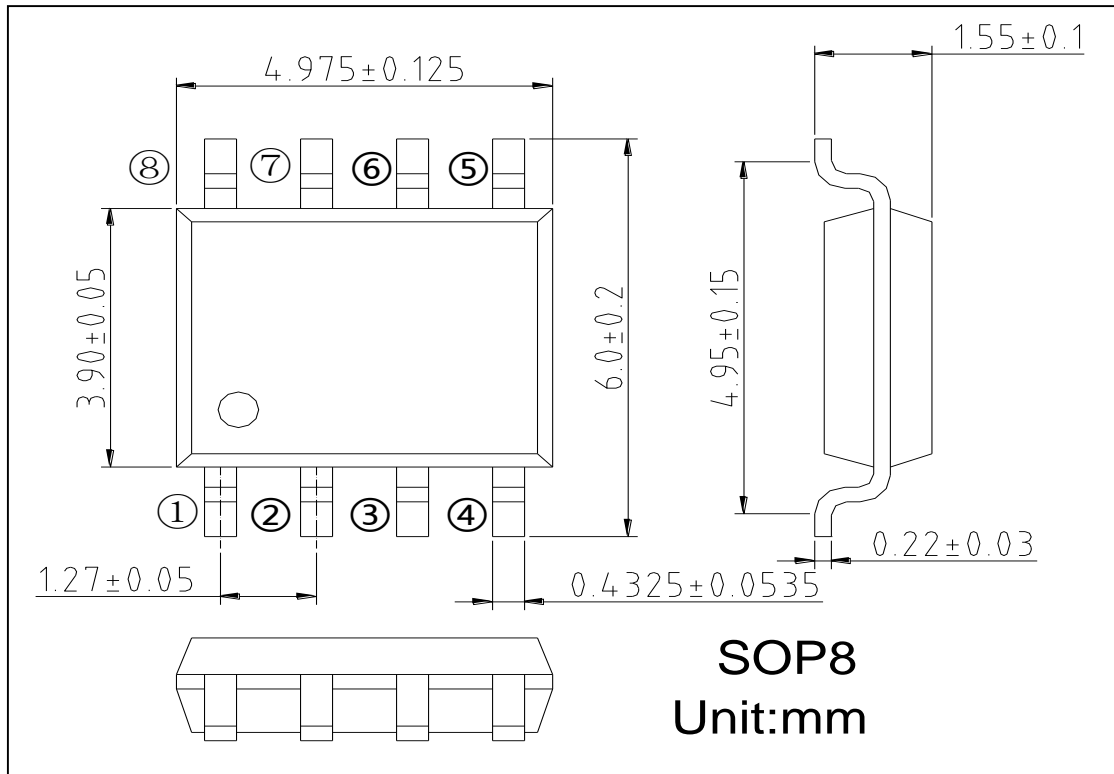
➤ **Typical Characteristics** ( $T_A=25^\circ\text{C}$  unless otherwise noted)







➤ Package Information



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