



# SSC8428GN2

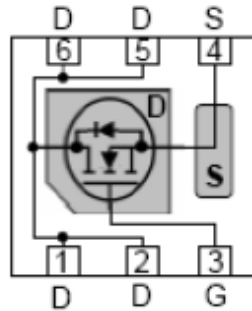
## N-Channel Enhancement Mode MOSFET

### ➤ Features

VDS	VGS	RDS(on) Typ.	ID
20V	±12V	11mR@10V	8A
		13mR@4V5	
		16mR@2V5	

### ➤ Pin configuration

Top view



### ➤ Description

Advance trench process technology.  
 High density cell design for ultralow on-resistance.  
 High power and current handling capability.  
 Fully characterized avalanche voltage and current.



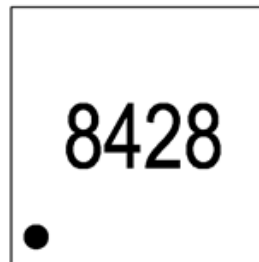
Bottom View

### ➤ Applications

- Load Switch
- Li-ion battery protection

### ➤ Ordering Information

Device	Package	Shipping
SSC8428GN2	DFN2x2	3000/Reel



Marking



➤ **Absolute Maximum Ratings**( $T_A=25^{\circ}\text{C}$  unless otherwise noted)

Symbol	Parameter	Ratings	Unit
$V_{DSS}$	Drain-to-Source Voltage	20	V
$V_{GSS}$	Gate-to-Source Voltage	$\pm 12$	V
$I_D$	Continuous Drain Current <sup>a</sup>	8	A
$I_{DM}$	Pulsed Drain Current <sup>b</sup>	30	A
$P_D$	Power Dissipation <sup>c</sup>	3.8	W
$P_{DSM}$	Power Dissipation <sup>a</sup>	1.8	W
$T_J$	Operation junction temperature	-25 to 85	$^{\circ}\text{C}$
$T_{STG}$	Storage temperature range	-55 to 150	$^{\circ}\text{C}$

➤ **Thermal Resistance Ratings**( $T_A=25^{\circ}\text{C}$  unless otherwise noted)

Symbol	Parameter	Typical	Maximum	Unit
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance <sup>a</sup>		75	$^{\circ}\text{C}/\text{W}$
$R_{\theta JC}$	Junction-to-Case Thermal Resistance		35	

Note:

- The value of  $R_{\theta JA}$  is measured with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz.copper, in a still air environment with  $T_A=25^{\circ}\text{C}$ . The value in any given application depends on the user is specific board design. The current rating is based on the  $t \leq 10\text{s}$  thermal resistance rating.
- Repetitive rating, pulse width limited by junction temperature.
- The power dissipation  $P_D$  is based on  $T_{J(MAX)}=150^{\circ}\text{C}$ , using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

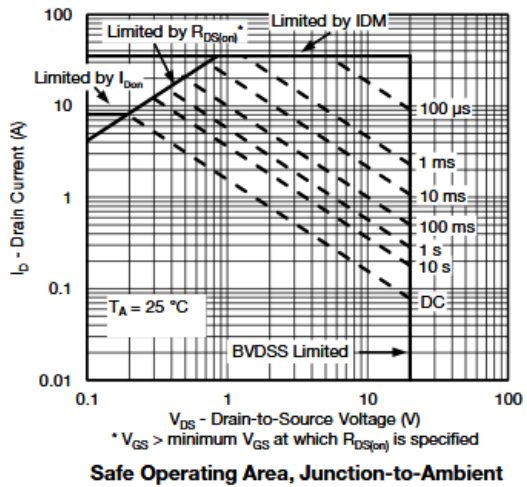
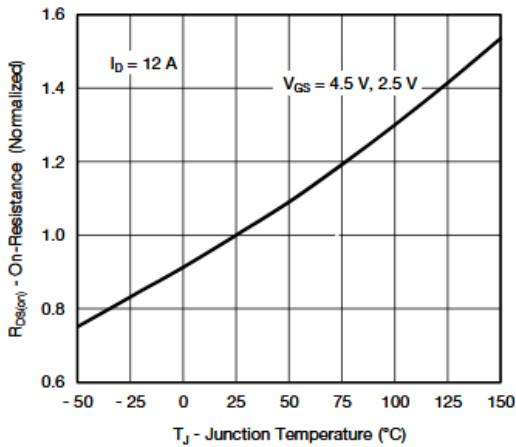
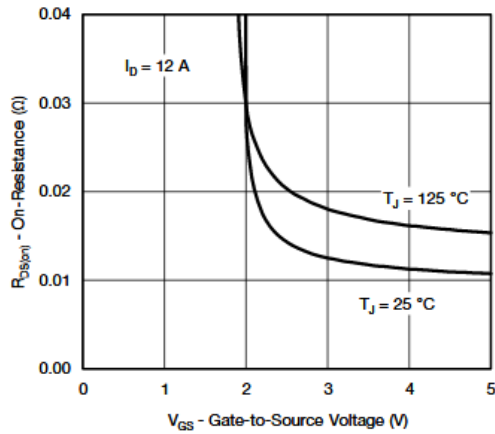
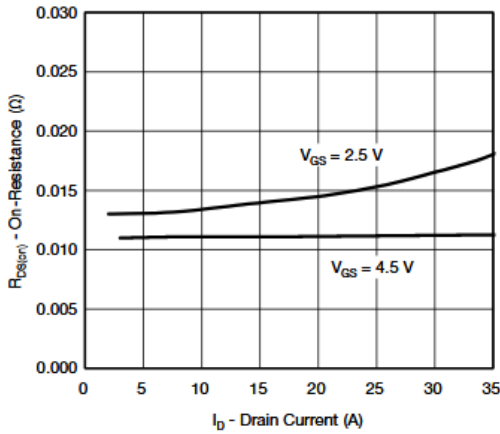
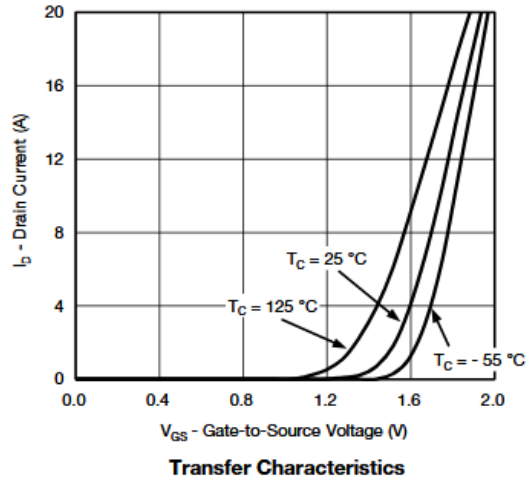
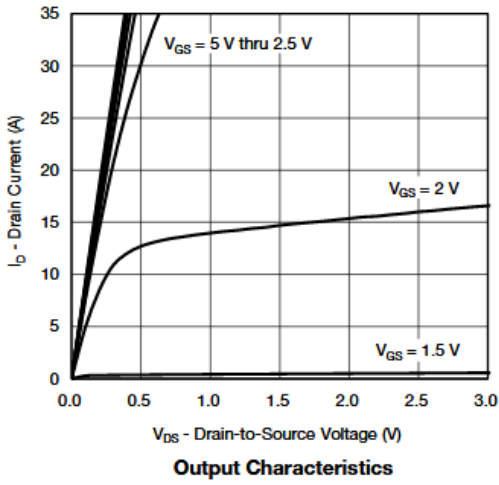


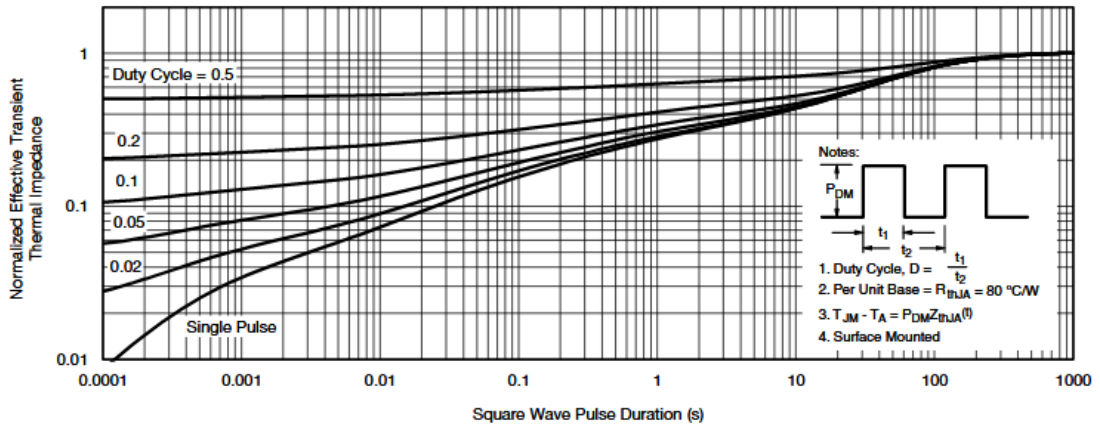
➤ **Electronics Characteristics**( $T_A=25^{\circ}\text{C}$  unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	20			V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	0.5	0.7	1	V
$R_{DS(on)}$	Drain-Source On- Resistance	$V_{GS}=10V, I_D=4.5A$		11	12	mR
		$V_{GS}=4.5V, I_D=3.5A$		13	15	
		$V_{GS}=2.5V, I_D=2.5A$		16	18	
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=16V, V_{GS}=0V$			1	$\mu A$
$I_{GSS}$	Gate-Source leak current	$V_{GS}=\pm 12V, V_{DS}=0V$			$\pm 100$	nA
$G_{FS}$	Transconductance	$V_{DS}=5V, I_D=4.5A$		10		S
$V_{SD}$	Forward Voltage	$V_{GS}=0V, I_S=0.5A$		0.8	1.3	V
$C_{iss}$	Input Capacitance	$V_{DS}=10V, V_{GS}=0V,$ $f=1MHz$		600		pF
$C_{oss}$	Output Capacitance			330		
$C_{rss}$	Reverse Transfer Capacitance			140		
$T_{D(ON)}$	Turn-on delay time	$V_{GEN}=4.5V, R_L=10R,$ $V_{DS}=10V, R_G=6R, I_D=1A$		7		ns
$T_r$	Rise Time			13		
$T_{D(OFF)}$	Turn-off delay time			48		
$T_f$	Fall Time			22		
$Q_g$	Total Gate charge	$V_{GS}=4.5V, V_{DS}=10V,$ $I_D=4A$		8.5		nC
$Q_{gs}$	Gate to Source charge			1.8		
$Q_{gd}$	Gate to Drain charge			2.2		



➤ Typical Characteristics ( $T_A=25^\circ\text{C}$  unless otherwise noted)

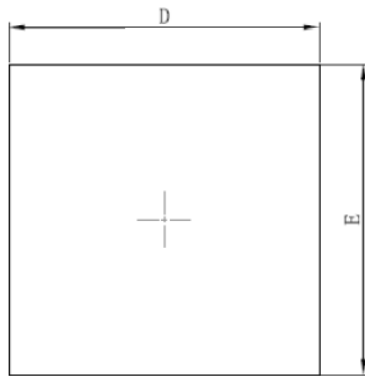




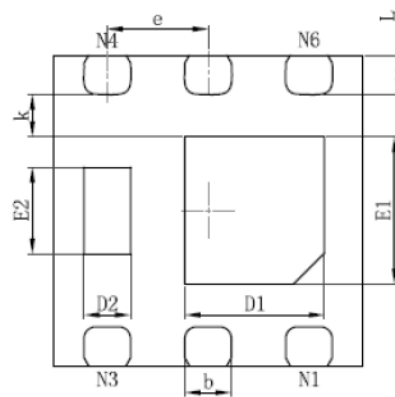
Normalized Thermal Transient Impedance, Junction-to-Ambient



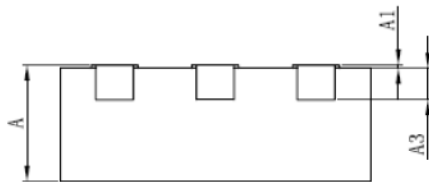
➤ Package Information



TOP VIEW



BOTTOM VIEW



SIDE VIEW

DFN2x2-6L

Symbol	Dimensions In Millimeters	
	Min.	Max.
A	0.700	0.800
A1	0.000	0.050
A3	0.203REF.	
D	1.924	2.076
E	1.924	2.076
D1	0.800	1.000
E1	0.850	1.050
D2	0.200	0.400
E2	0.460	0.660
k	0.200MIN.	
b	0.250	0.350
e	0.650TYP.	
L	0.174	0.326



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