



## SSC2314GS6A

### N-Channel Enhancement Mode MOSFET

#### ➤ Features

VDS	VGS	RDS(on) Typ.	ID
20V	±12V	22mR@4V5	6A
		25mR@2V5	
		38mR@1V8	

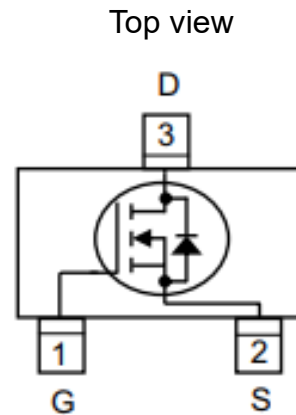
#### ➤ Description

This device is produced with high cell density DMOS trench technology, which is especially used to minimize on-state resistance. This device particularly suits low voltage applications such as portable equipment, power management and other battery powered circuits, and low in-line power dissipation are needed in a very small outline surface mount package. Excellent thermal and electrical capabilities.

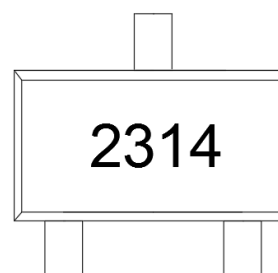
#### ➤ Applications

- Load Switch
- Portable Devices
- DCDC conversion

#### ➤ Pin configuration



SOT23-3



Marking

#### ➤ Ordering Information

Device	Package	Shipping
SSC2314GS6A	SOT23-3	3000/Reel



➤ **Absolute Maximum Ratings**( $T_A=25^{\circ}\text{C}$  unless otherwise noted)

Symbol	Parameter	Ratings	Unit
$V_{DSS}$	Drain-to-Source Voltage	20	V
$V_{GSS}$	Gate-to-Source Voltage	$\pm 12$	V
$I_D$	Continuous Drain Current <sup>a</sup>	6	A
$I_{DM}$	Pulsed Drain Current <sup>b</sup>	18	A
$P_D$	Power Dissipation <sup>c</sup>	1.2	W
$P_{DSM}$	Power Dissipation <sup>a</sup>	0.6	W
$T_J$	Operation junction temperature	-55 to 150	$^{\circ}\text{C}$
$T_{STG}$	Storage temperature range	-55 to 150	$^{\circ}\text{C}$

➤ **Thermal Resistance Ratings**( $T_A=25^{\circ}\text{C}$  unless otherwise noted)

Symbol	Parameter	Typical	Maximum	Unit
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance <sup>a</sup>		220	$^{\circ}\text{C}/\text{W}$
$R_{\theta JC}$	Junction-to-Case Thermal Resistance		110	

Note:

- The value of  $R_{\theta JA}$  is measured with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz.copper,in a still air environment with  $T_A=25^{\circ}\text{C}$ .The value in any given application depends on the user is specific board design. The current rating is based on the  $t \leq 10\text{s}$  thermal resistance rating.
- Repetitive rating, pulse width limited by junction temperature.
- The power dissipation  $P_D$  is based on  $T_{J(MAX)}=150^{\circ}\text{C}$ , using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

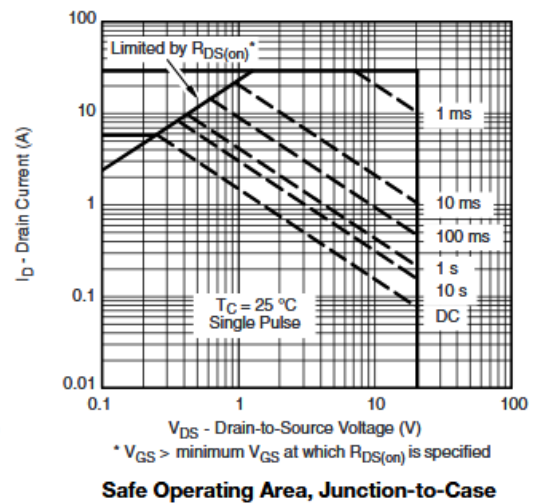
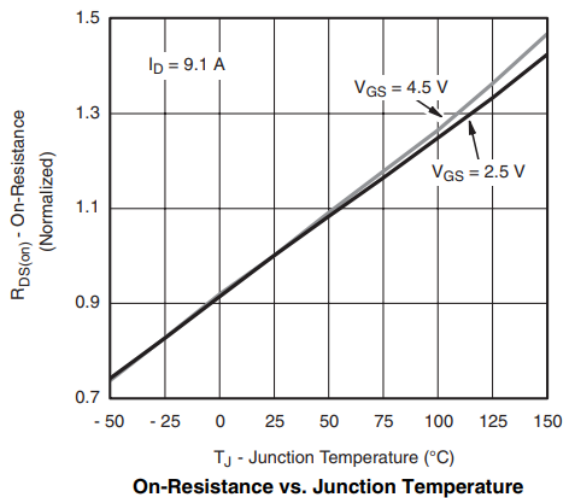
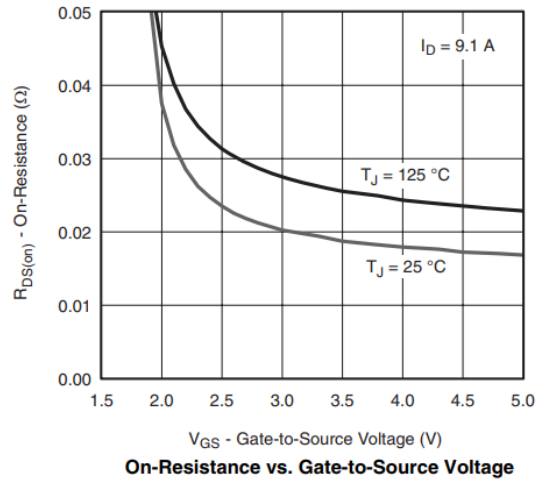
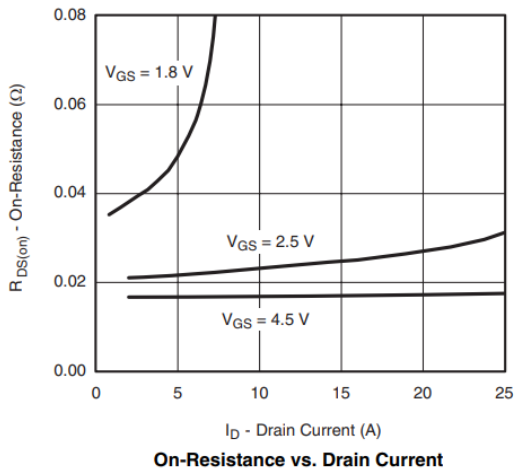
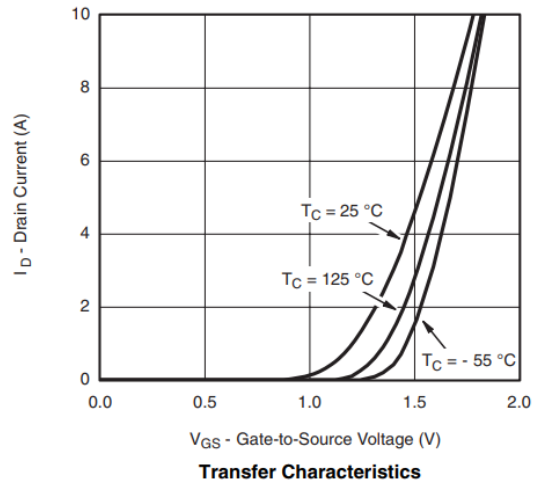
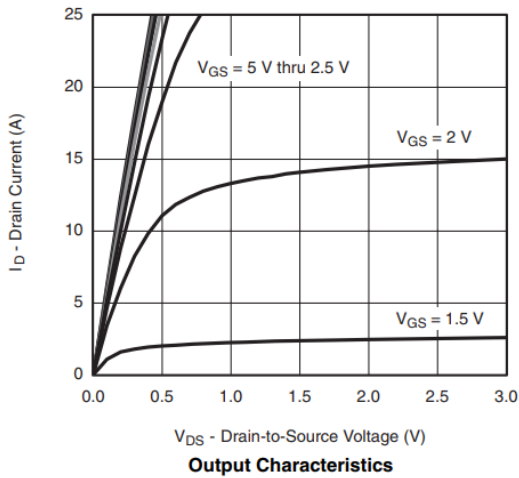


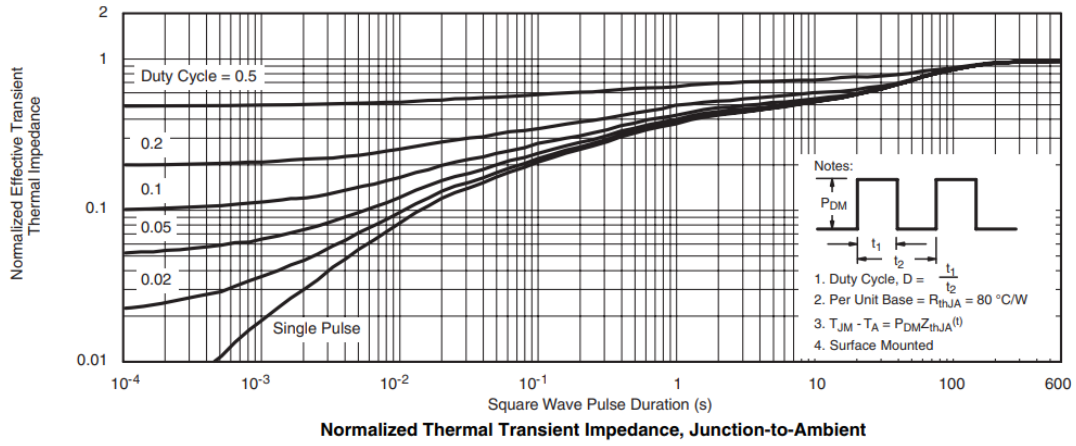
➤ **Electronics Characteristics**( $T_A=25^{\circ}\text{C}$  unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	20			V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	0.4	0.6	0.9	V
$R_{DS(on)}$	Drain-Source On- Resistance	$V_{GS}=4.5V, I_D=5A$		22	31	mR
		$V_{GS}=2.5V, I_D=3.5A$		25	37	
		$V_{GS}=1.8V, I_D=2.8A$		38	50	
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=20V, V_{GS}=0V$			1	$\mu A$
$I_{GSS}$	Gate-Source leak current	$V_{GS}=\pm 12V, V_{DS}=0V$			$\pm 100$	nA
$G_{FS}$	Transconductance	$V_{DS}=5V, I_D=3.6A$		7	14	S
$V_{SD}$	Forward Voltage	$V_{GS}=0V, I_S=1.1A$		0.8	1.15	V
$C_{iss}$	Input Capacitance	$V_{DS}=10V, V_{GS}=0V, f=1MHz$		469		pF
$C_{oss}$	Output Capacitance			81		
$C_{rss}$	Reverse Transfer Capacitance			49		
$T_{D(ON)}$	Turn-on delay time		$V_{GS}=4.5V,$ $V_{DS}=5V, R_G=6R, I_D=3.6A$		15	
$T_r$	Rise Time			10		
$T_{D(OFF)}$	Turn-off delay time			60		
$T_f$	Fall Time			22		
$Q_g$	Total Gate charge	$V_{GS}=4.5V, V_{DS}=10V, I_D=4A$		11		nC
$Q_{gs}$	Gate to Source charge			1.1		
$Q_{gd}$	Gate to Drain charge			3.3		



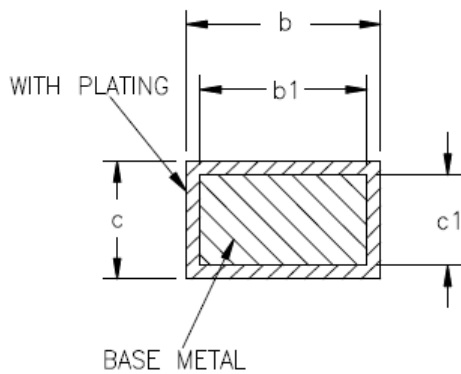
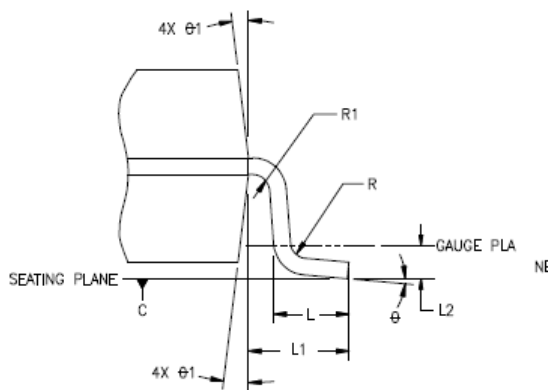
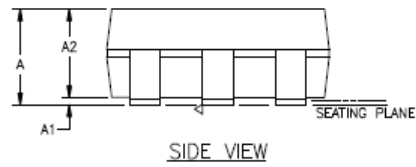
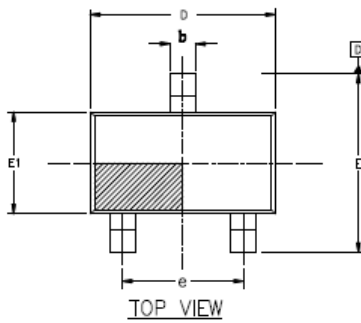
➤ **Typical Characteristics** ( $T_A=25^\circ\text{C}$  unless otherwise noted)







➤ Package Information



SYMBOL	MIN	NOM	MAX
A	--	--	1.35
A1	0	--	0.15
A2	1.0	1.1	1.2
b	0.35	--	0.45
b1	0.32	--	0.38
c	0.14	--	0.20
c1	0.14	0.15	0.16
D	2.82	2.92	3.02
E	2.60	2.80	3.00
E1	1.526	1.626	1.726
e	1.8	1.9	2.0
L	0.35	0.45	0.6
L1	0.6REF		
L2	0.25REF		
R	0.1	--	--
R1	0.1	--	--
θ	0°	4°	8°
θ1	5°	10°	15°

**NOTES:**  
 1. ALL DIMENSIONS REFER TO JEDEC STANDARD MO-178  
 2. DIMENSION D DOES NOT INCLUDE MOLD FLASH  
 3. DIMENSION E1 DOES NOT INCLUDE MOLD FLASH  
 4. FLASH OR PROTRUSION SHALL NOT EXCEED 0.25mm PER SIDE.

SOT23-3L



➤ **History Version**

V1.0	Product datasheet	2017-07-01
V2.1	Update POD	2020-08-28

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