SSC8632GN4

N- and P-Channel Complementary, MOSFET

➢ Features

N-Channel

VDS	VGS	RDSON Typ.	ID
30V	±20V	16mR@10V	8A
		20mR@4V5	

P-Channel

VDS	VGS	RDSON Typ.	ID
-30V	±20V	42mR@-10V	-6A
		60mR@-4V5	

➢ Description

SSC8632GN4 uses advanced trench technology to provide excellent RDSON and low gate charge. The complementary MOSFETS may be used to form a level shifted high side switch, and for a host of other applications.

➢ Applications

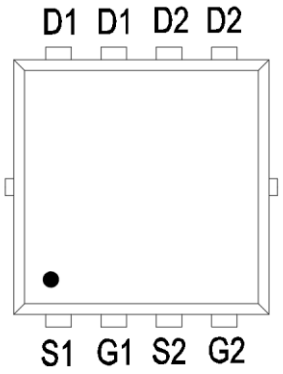
- Inverter
- CCFL Driver

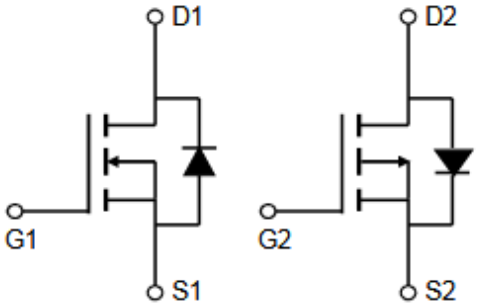
➢ Ordering Information

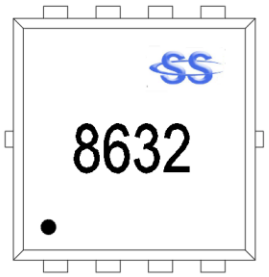
Device	Package	Shipping
SSC8632GN4	PDFN3.3X3.3	5000/Reel

➢ Pin configuration

Top view







Marking

➢ Absolute Maximum Ratings(T_A=25℃ unless otherwise noted)

Symbol	Parameter		N-Channel	P-Channel	Unit
V_{DSS}	Drain-to-Source Voltage		30	-30	V
V_{GSS}	Gate-to-Source Voltage		±20	±20	V
I_D	Continuous Drain Current [a]	TA=25C°	8	-6	A
		TA=70C°	6	-5	A
I_{DM}	Pulsed Drain Current [b]		32	-24	A
P_{DSM}	Power Dissipation [a]	TC=25C°	20		W
I_{AS}	Avalanche Current [b] L=0.1mH Single Pulse		20	18	A
E_{AS}	Avalanche Energy [b] L=0.1mH Single Pulse		20	16	mJ
P_D	Power Dissipation [c]	TA=25C°	2.6		W
		TA=70C°	1.6		W
T_J	Operation junction temperature		-55 to 150		℃
T_{STG}	Storage temperature range		-55 to 150		℃

➢ Thermal Resistance Ratings(T_A=25℃ unless otherwise noted)

Symbol	Parameter	Typical	Maximum	Unit
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance [a]		48	℃/W
$R_{\theta JC}$	Junction-to-Case Thermal Resistance		6.25	

Note:

a. The value of $R_{\theta JA}$ is measured with the device mounted on 1 in^2 FR-4 board with 2oz.copper,in a still air environment with T_A=25C°.The value in any given application depends on the user is specific board design. The current rating is based on the t ≤ 10s thermal resistance rating.

b. Repetitive rating, pulse width limited by junction temperature.

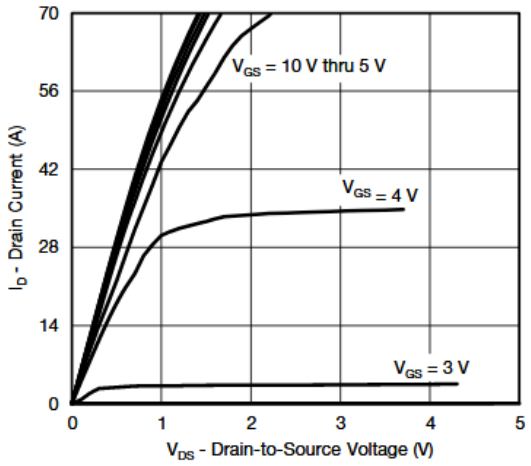
c. The power dissipation P_D is based on $T_{J(MAX)}$=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

➢ **Electronics Characteristics**(T_A=25℃ unless otherwise noted)

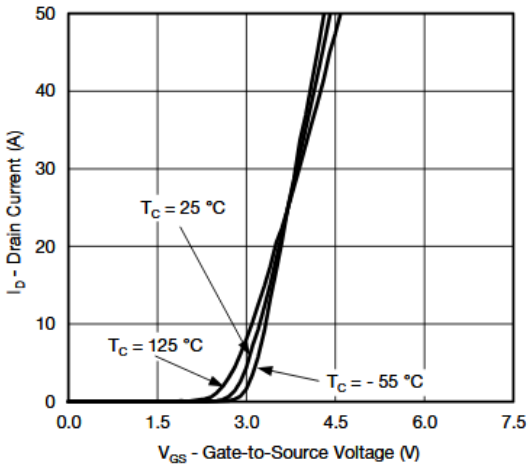
Symbol	Parameter	Test Conditions		Min	Typ.	Max	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	VGS=0V,ID=250uA	N-CH	30			V
		VGS=0V,ID=-250uA	P-CH	-30			
$V_{GS\ (th)}$	Gate Threshold Voltage	VDS=VGS,ID=250uA	N-CH	1	1.4	3	V
		VDS=VGS,ID=-250uA	P-CH	-1	-1.5	-3	
$R_{DS(on)}$	Drain-Source On-Resistance	VGS=10V,ID=6A	N-CH		16	24	mR
		VGS=10V,ID=-4A	P-CH		42	60	
		VGS=4.5V,ID=5A	N-CH		20	32	
		VGS=-4.5V,ID=-3A	P-CH		60	80	
I_{DSS}	Zero Gate Voltage Drain Current	VDS=24V,VGS=0V	N-CH			1	uA
		VDS=-24V,VGS=0V	P-CH			-1	
I_{GSS}	Gate-Source leak current	VGS=±20V,VDS=0V	N-CH			±100	nA
		VGS=±20V,VDS=0V	P-CH			±100	
G_{FS}	Forward Transconductance	VDS=5V,ID=6A	N-CH		10		S
		VDS=-5V,ID=-4A	P-CH		15		
V_{SD}	Forward Voltage	VGS=0V,IS=1A	N-CH		0.78	1.3	V
		VGS=0V,IS=-1A	P-CH		-0.77	-1.3	
Ciss	Input Capacitance	**NMOS:** VDS=15V, VGS=0V, f=1MHZ **PMOS:** VDS=-15V, VGS=0V, f=1MHZ	N-CH		540		pF
			P-CH		550		
Coss	Output Capacitance		N-CH		82		
			P-CH		87		
Crss	Reverse Transfer Capacitance		N-CH		28		
			P-CH		31		

Qg	Total Gate Charge	**NMOS:** VDS=15V, VGS=10V, ID=8A **PMOS:** VDS=-15V, VGS=-10V, ID=-6A	N-CH		10		nC
			P-CH		9		
Qgs	Gate Source Charge		N-CH		2.2		
			P-CH		2.3		
Qgd	Gate Drain Charge		N-CH		1.1		
			P-CH		1.9		
$T_{D(ON)}$	Turn-on delay time	**NMOS:** VDS=15V, VGS=10V, RL=10R, RGEN=6R **PMOS:** VDS=-15V, VGS=-10V, RL=10R, RGEN=6R	N-CH		9		ns
			P-CH		13		
Tr	Rise time		N-CH		12		
			P-CH		15		
$T_{D(OFF)}$	Turn-off delay time		N-CH		26		
			P-CH		21		
Tf	Fall time		N-CH		18		
			P-CH		14		

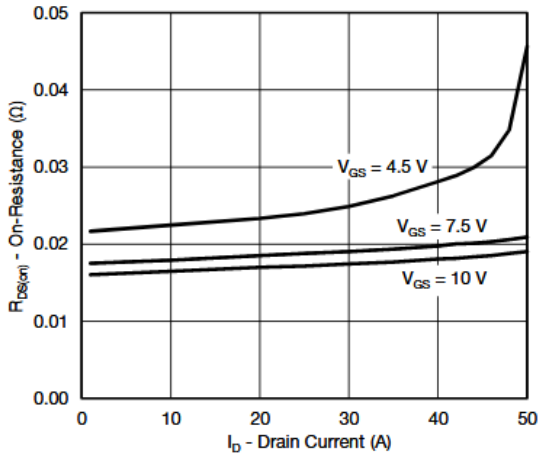
➢ N-Channel Typical Characteristics (TA=25℃ unless otherwise noted)



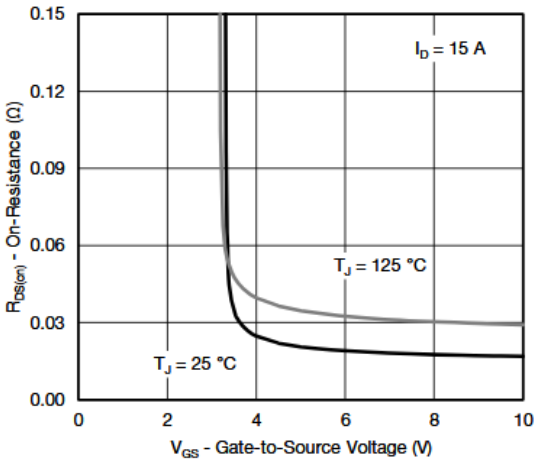
Output Characteristics



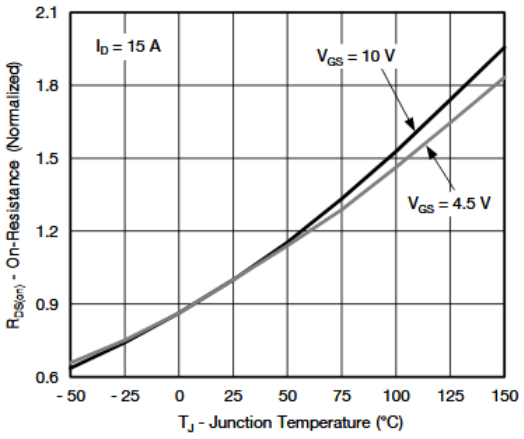
Transfer Characteristics



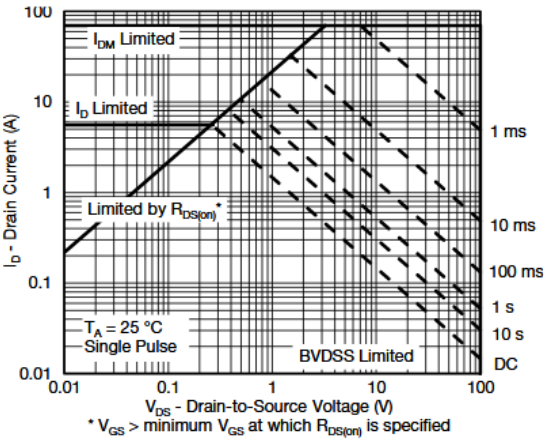
On-Resistance vs. Drain Current



On-Resistance vs. Gate-to-Source Voltage

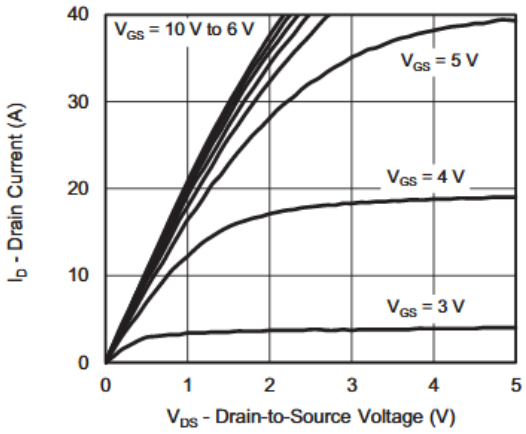


On-Resistance vs. Junction Temperature

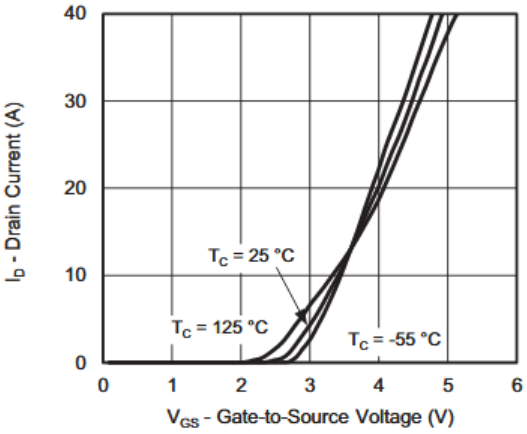


Safe Operating Area, Junction-to-Ambient

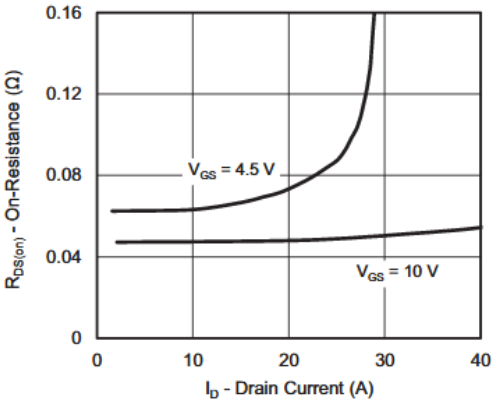
➢ P-Channel Typical Characteristics(TA=25℃ unless otherwise noted)



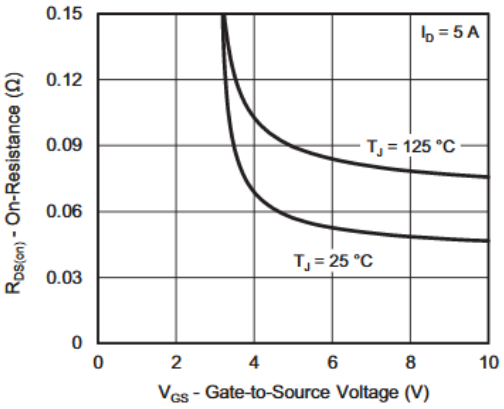
Output Characteristics



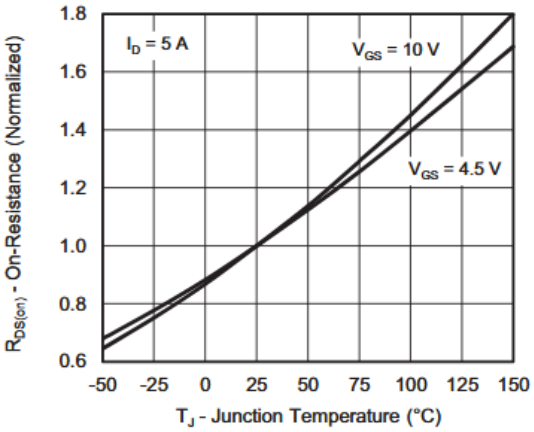
Transfer Characteristics



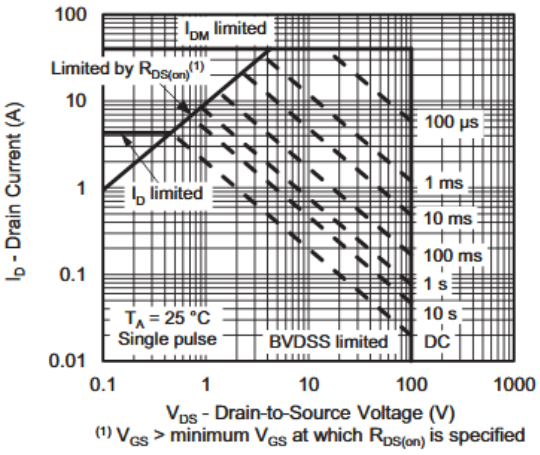
On-Resistance vs. Drain Current and Gate Voltage



On-Resistance vs. Gate-to-Source Voltage

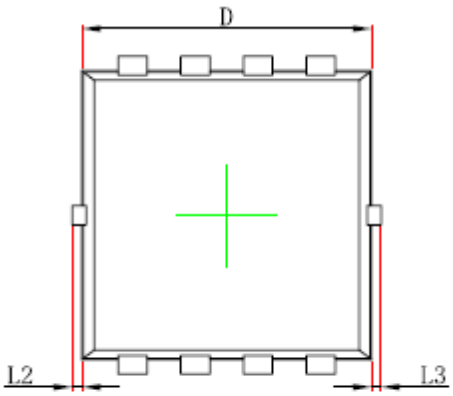


On-Resistance vs. Junction Temperature

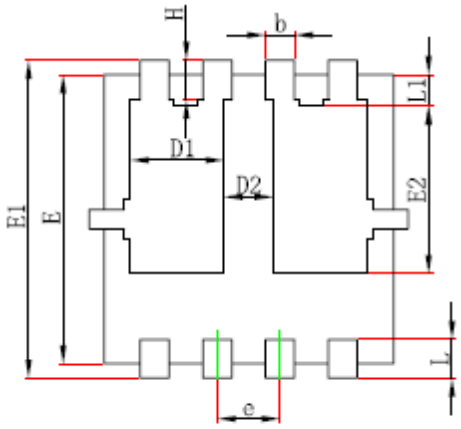


Safe Operating Area, Junction-to-Ambient

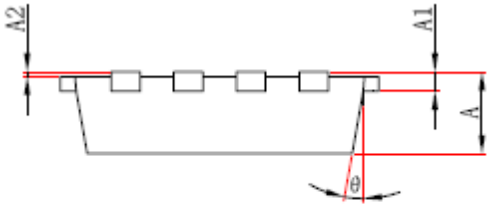
➢ Package Information



Top View
[顶视图]



Bottom View
[背视图]



Side View
[侧视图]

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.650	0.850	0.026	0.033
A1	0.152 REF.		0.006 REF.	
A2	0~0.05		0~0.002	
D	2.900	3.100	0.114	0.122
D1	0.935	1.135	0.037	0.045
D2	0.280	0.480	0.011	0.019
E	2.900	3.100	0.114	0.122
E1	3.150	3.450	0.124	0.136
E2	1.535	1.935	0.060	0.076
b	0.200	0.400	0.008	0.016
e	0.550	0.750	0.022	0.030
L	0.300	0.500	0.012	0.020
L1	0.180	0.480	0.007	0.019
L2	0~0.100		0~0.004	
L3	0~0.100		0~0.004	
H	0.315	0.515	0.012	0.020
θ	9°	13°	9°	13°

DISCLAIMER

AFSEMI RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. AFSEMI DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICIENCE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

THE GRAPHS PROVIDED IN THIS DOCUMENT ARE STATISTICAL SUMMARIES BASED ON A LIMITED NUMBER OF SAMPLES AND ARE PROVIDED FOR INFORMATIONAL PURPOSE ONLY. THE PERFORMANCE CHARACTERISTICS LISTED IN THEM ARE NOT TESTED OR GUARANTEED. IN SOME GRAPHS, THE DATA PRESENTED MAY BE OUTSIDE THE SPECIFIED OPERATING RANGE (E.G. OUTSIDE SPECIFIED POWER SUPPLY RANGE) AND THEREFORE OUTSIDE THE WARRANTED RANGE.