



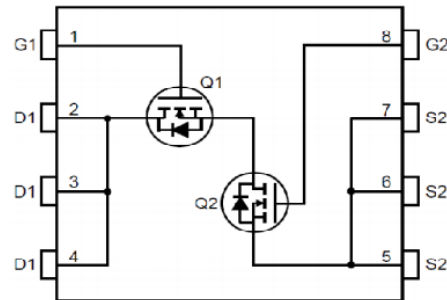
SSC8330GQ4

Dual Asymmetric N-Channel Enhancement Mode MOSFET

➤ **Features**

	VDS	VGS	RDSON Typ.	ID
Q1	30V	±20V	7.4mΩ@10V	33A
			8.1mΩ@4V5	
Q2	30V	±20V	5.5mΩ@10V	35A
			9.5mΩ@4V5	

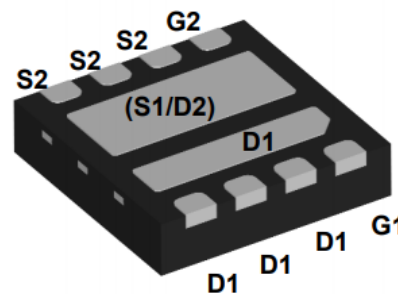
➤ **Pin configuration**



Top View

➤ **Description**

This device uses advanced trench technology to provide excellent RDSON and low gate charge. This device is suitable for use as a load switch or in PWM applications.



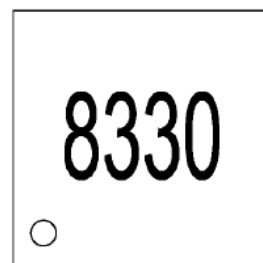
Bottom View

➤ **Applications**

- Isolated DC/DC Converters
- DC/DC conversion in computing
- Load Switch

➤ **Ordering Information**

Device	Package	Shipping
SSC8330GQ4	DFN3X3-8L	5000/Reel



Marking

➤ **Absolute Maximum Ratings** ($T_A=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter		Ratings		Unit
			Q1	Q2	
V_{DSS}	Drain-to-Source Voltage		30	30	V
V_{GSS}	Gate-to-Source Voltage		± 20	± 20	V
I_D	Continuous Drain Current	TC=25°C	33	35	A
		TC=100°C	18	20	A
I_{DM}	Pulsed Drain Current ^b		132	144	A
I_{DSM}	Continuous Drain Current ^a	TA=25°C	11	12.6	A
		TA=70°C	8.3	9.1	A
P_D	Power Dissipation ^c	TC=25°C	21	20.1	W
		TC=100°C	8.3	8.3	W
P_{DSM}	Power Dissipation ^a	TA=25°C	2.3	2.3	W
		TA=70°C	1.5	1.5	W
I_{AS}	Avalanche Current		19	25	A
E_{AS}	Avalanche Energy, L=0.5mH		90	156	mJ
T_J	Operation junction temperature		-55 to 150		°C
T_{STG}	Storage temperature range		-55 to 150		°C

➤ **Thermal Resistance Ratings** ($T_A=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Typical	Maximum		Unit
			Q1	Q2	
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance ^a		55	55	°C/W
$R_{\theta JC}$	Junction-to-Case Thermal Resistance		6.5	6	

Note:

- The value of $R_{\theta JA}$ is measured with the device mounted on 1 in² FR-4 board with 2oz.copper, in a still air environment with $T_A=25^\circ\text{C}$. The value in any given application depends on the user's specific board design. The current rating is based on the $t \leq 10\text{s}$ thermal resistance rating.
- Repetitive rating, pulse width limited by junction temperature.
- The power dissipation P_D is based on $T_{J(MAX)}=150^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.



➤ **Q1 Electronics Characteristics**($T_A=25^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	30			V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	1	1.65	2.1	V
$R_{DS(on)}$	Drain-Source On- Resistance	$V_{GS}=10V, I_D=15A$		7.4	13	m Ω
		$V_{GS}=4.5V, I_D=12A$		8.1	16	
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=24V, V_{GS}=0V$			1	μA
I_{GSS}	Gate-Source leak current	$V_{GS}=\pm 20V, V_{DS}=0V$			± 100	nA
V_{SD}	Forward Voltage	$V_{GS}=0V, I_S=0.5A$		0.8	1.3	V
G_{FS}	Transconductance	$V_{DS}=15V, I_D=10A$		50		S
C_{iss}	Input Capacitance	$V_{DS}=15V, V_{GS}=0V, f=1MHz$		800		pF
C_{oss}	Output Capacitance			255		
C_{rss}	Reverse Transfer Capacitance			75		
$T_{D(ON)}$	Turn-on delay time	$V_{GS}=10V,$ $V_{DS}=15V, R_G=3\Omega, R_L=2.3\Omega$		15		ns
T_r	Rise time			9		
$T_{D(OFF)}$	Turn-off delay time			55		
T_f	Fall time			16		
Q_g	Total Gate charge	$V_{GS}=10V, V_{DS}=15V, I_D=13A$		8		nC
Q_{gs}	Gate to Source charge			1.1		
Q_{gd}	Gate to Drain charge			2.2		

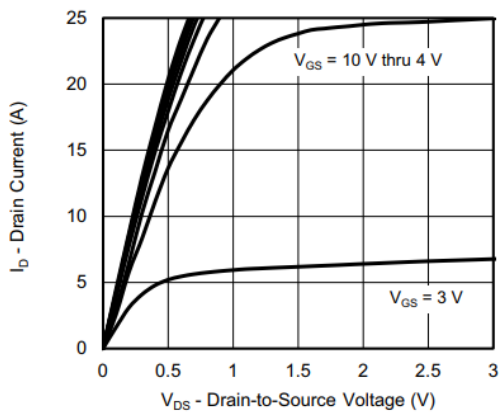


➤ **Q2 Electronics Characteristics**($T_A=25^{\circ}\text{C}$ unless otherwise noted)

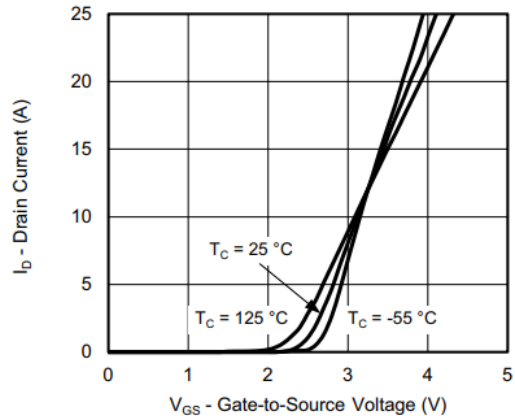
Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	30			V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	1	1.55	3	V
$R_{DS(on)}$	Drain-Source On- Resistance	$V_{GS}=10V, I_D=15A$		5.5	11	m Ω
		$V_{GS}=4.5V, I_D=12A$		9.5	14	
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=24V, V_{GS}=0V$			1	μA
I_{GSS}	Gate-Source leak current	$V_{GS}=\pm 20V, V_{DS}=0V$			± 100	nA
V_{SD}	Forward Voltage	$V_{GS}=0V, I_S=1A$		0.8	1.5	V
G_{FS}	Transconductance	$V_{DS}=15V, I_D=10A$		60		S
C_{iss}	Input Capacitance	$V_{DS}=15V, V_{GS}=0V, f=1MHz$		1000		pF
C_{oss}	Output Capacitance			269		
C_{rss}	Reverse Transfer Capacitance			105		
$T_{D(ON)}$	Turn-on delay time	$V_{GS}=10V,$ $V_{DS}=15V, R_G=3\Omega, R_L=2.3\Omega$		8		ns
T_r	Rise time			4		
$T_{D(OFF)}$	Turn-off delay time			18		
T_f	Fall time			6		
Q_g	Total Gate charge	$V_{GS}=10V, V_{DS}=15V, I_D=13A$		15		nC
Q_{gs}	Gate to Source charge			2.2		
Q_{gd}	Gate to Drain charge			3.3		



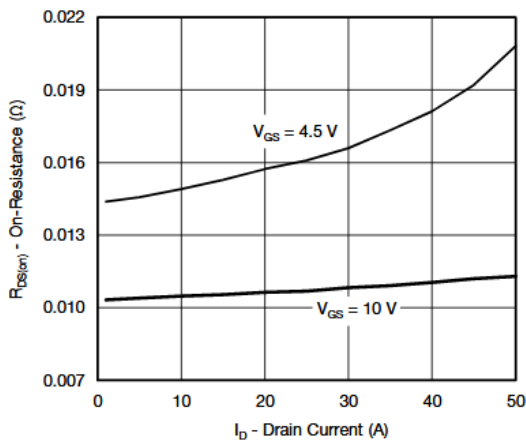
➤ Q1 Typical Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)



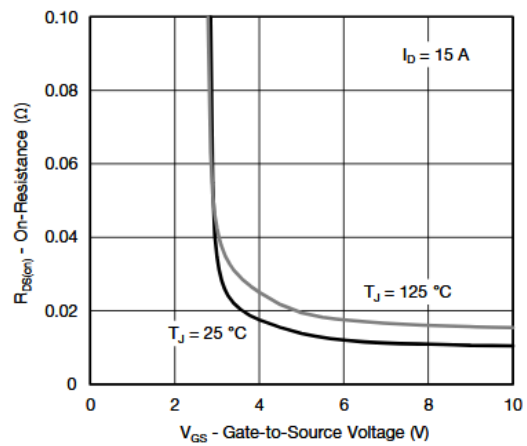
Output Characteristics



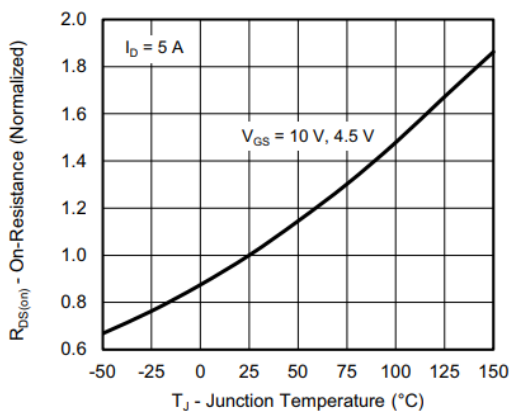
Transfer Characteristics



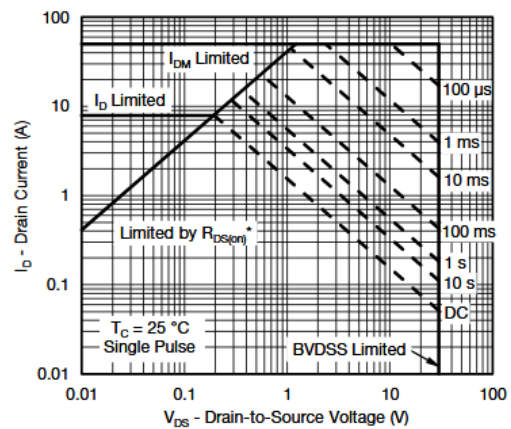
On-Resistance vs. Drain Current and Gate Voltage



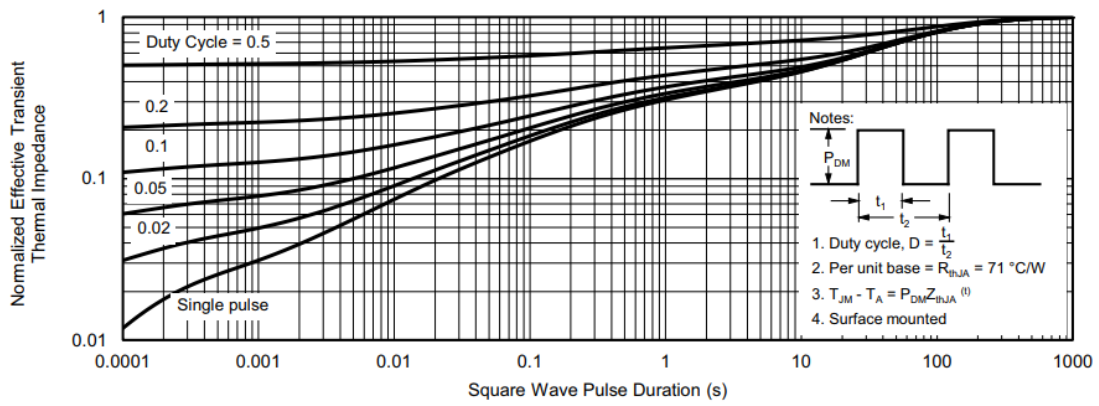
On-Resistance vs. Gate-to-Source Voltage



On-Resistance vs. Junction Temperature



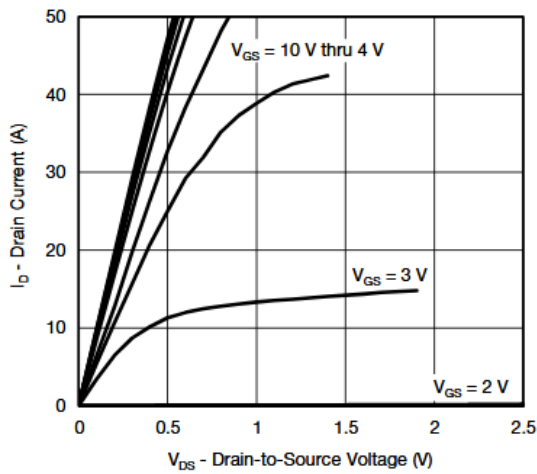
Safe Operating Area, Junction-to-Ambient



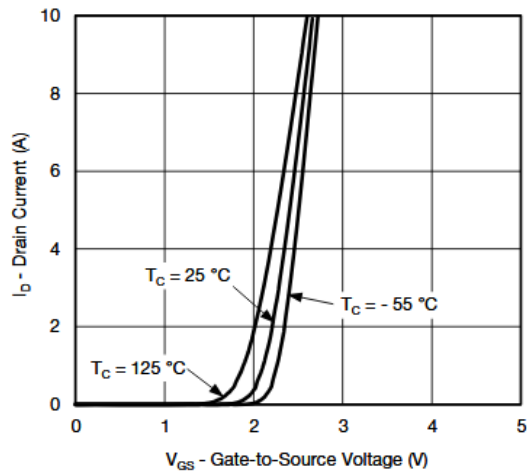
Normalized Thermal Transient Impedance, Junction-to-Ambient



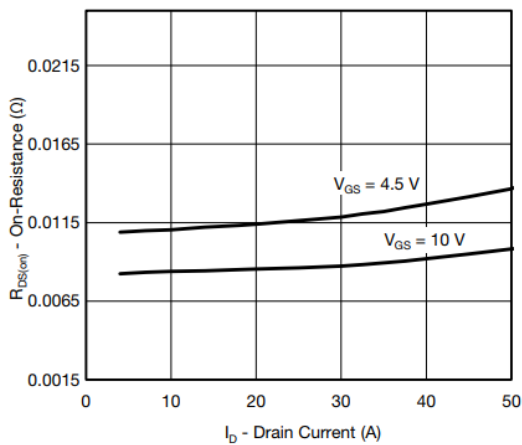
➤ Q2 Typical Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)



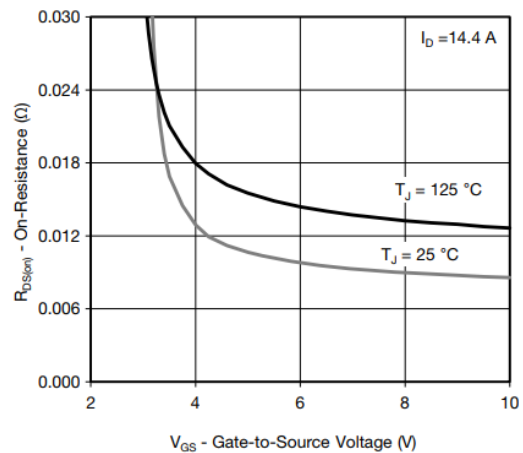
Output Characteristics



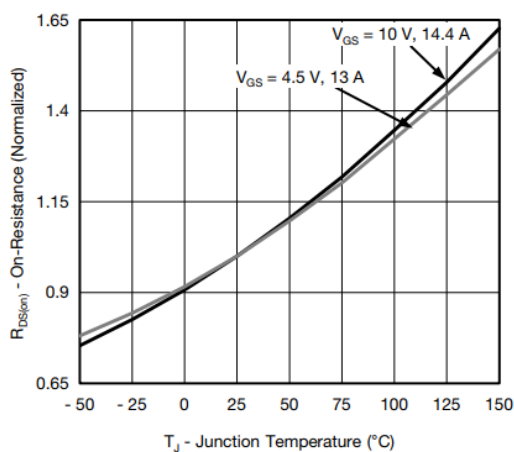
Transfer Characteristics



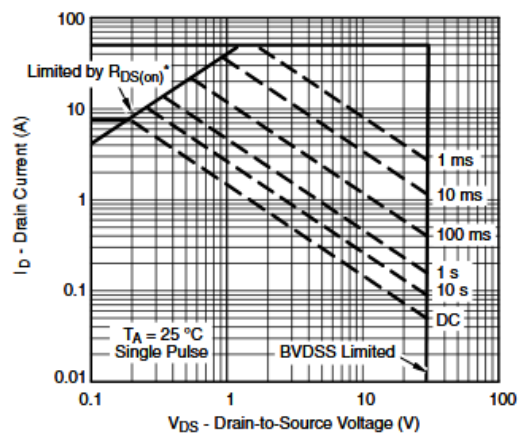
On-Resistance vs. Drain Current



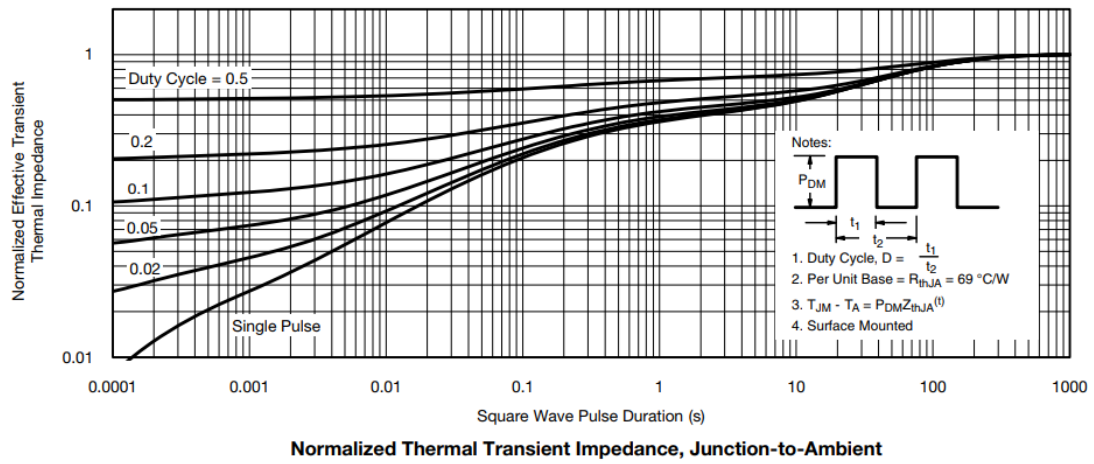
On-Resistance vs. Gate-to-Source Voltage

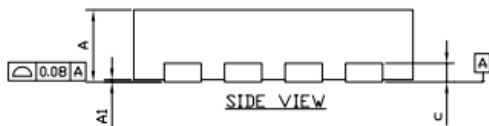
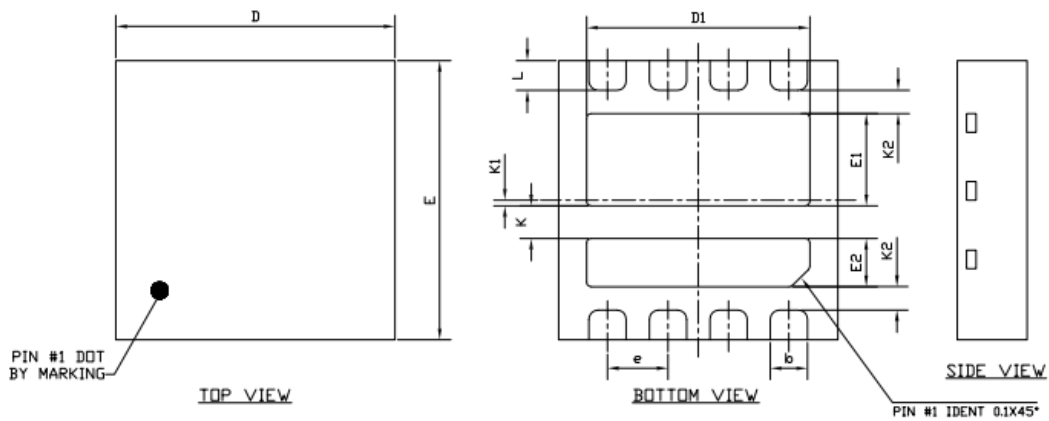


On-Resistance vs. Junction Temperature



Safe Operating Area, Junction-to-Ambient



➤ Package Information

DFN3X3-8L

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.75	0.80	0.028	0.030	0.032
A1	0.00	---	0.05	0.000	---	0.002
c	0.203 REF.			0.008 REF.		
b	0.35	0.40	0.45	0.014	0.016	0.018
D	2.90	3.00	3.10	0.114	0.118	0.122
D1	2.30	2.40	2.50	0.090	0.094	0.098
E	2.90	3.00	3.10	0.114	0.118	0.122
E1	0.89	0.99	1.09	0.035	0.039	0.043
E2	0.42	0.52	0.62	0.016	0.020	0.024
e	0.65 BSC			0.026 BSC		
L	0.27	0.32	0.37	0.011	0.013	0.015
K	0.35 REF.			0.014 REF.		
K1	0.06 REF.			0.002 REF.		
K2	0.25 REF.			0.010 REF.		



➤ **History Version**

V3.0		
V3.1	Change ID Change Q1/Q2 Rdson Typ.	2023-11-07

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