

SSC8219GN4

P-Channel Enhancement Mode MOSFET

> Features

V _{DS}	V _{GS}	R _{DS(ON)} Typ.	l _D
-16V	+12V	7.8mΩ@-4.5V	-45A
-100	<u> </u>	10.2mΩ@-2.5V	-43/

Description

The SSC8219GN4 is P-Channel enhancement mode MOSFET. Uses trench Technology and design to provide excellent RDSON with low gate charge. This device is suitable for use in DC - DC conversion, power switch and charging circuit.

100% UIS + ΔVDS + Rg Tested!

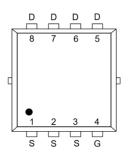
> Applications

- Inverter
- DC-DC Converter
- Half and Full Bridge Topology
- Motor Drive Control

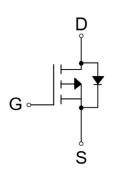
Ordering Information

Device	Package	Shipping	
SSC8219GN4	PDFN3.3X3.3-8L	5000/Reel	

Pin configuration



PDFN3.3x3.3-8L (Top View)



Pin Configuration



Marking

(XXYY: Internal Traceability Code)



➤ Absolute Maximum Ratings (T_A=25°C unless otherwise noted)

Symbol	Parameter		Ratings	Unit
V _{DSS}	Drain-to-Source Voltage		-16	V
V _{GSS}	Gate-to-Source Volt	Gate-to-Source Voltage		V
	I_D Continuous Drain Current b $T_C = 25^{\circ}C$ $T_C = 100^{\circ}C$	T _C = 25°C	-45	А
ID		-24	А	
I _{DM}	Pulsed Drain Curre	nt ^b	-178	А
•	Continuous Drain Current ^a	T _A = 25℃	-16	А
ldsм		T _A = 70°C	-11.4	А
D	David Distriction	T _C = 25°C	25	W
P_D	Power Dissipation ^c	T _C = 100°C Trent b $T_A = 25°C$ $T_A = 70°C$ $T_C = 25°C$ $T_C = 100°C$ $T_A = 25°C$ $T_A = 70°C$ $= 0.5mH$	10	W
Danie	Davis Diadratica 2	T _A = 25°C	3.2	W
P _{DSM}	Power Dissipation ^a	T _A = 70°C	2	W
I _{AS}	Avalanche Current b L = 0.5mH		-19	А
E _{AS}	Avalanche Energy b L = 0.5mH		90	mJ
TJ	Operation junction temperature		-55 to 150	$^{\circ}$
T _{STG}	Storage temperature range		-55 to 150	$^{\circ}$ C

➤ Thermal Resistance Ratings (T_A=25°C unless otherwise noted)

Symbol	Parameter	Ratings	Unit
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance a	40	°C ////
Rejc	Junction-to-Case Thermal Resistance	3.7	°C/W

Note:

- a. The value of R_{θJA} is measured with the device mounted on 1 in² FR-4 board with 2oz.copper,in a still air environment with T_A=25 °C. The value in any given application depends on the user is specific board design. The current rating is based on the t≤10s thermal resistance rating.
- b. Repetitive rating, pulse width limited by junction temperature.
- c. The power dissipation P_D is based on T_{J(MAX)}=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.
- d. The maximum current rating is package limited.

SSC-V1.2 www.sscsemi.com Analog Future



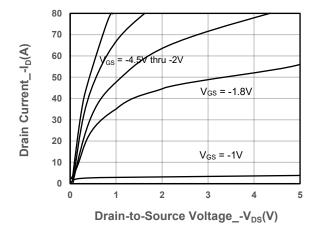


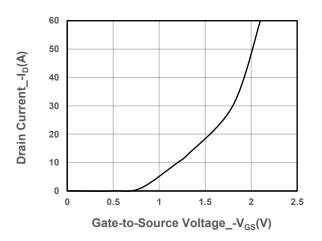
\succ Electrical Characteristics (T_A=25°C unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = -250uA	-16			V
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = -250uA$	-0.4	-0.6	-1	V
Drain-Source On-Resistance	R _{DS(on)}	V _{GS} = -4.5V, I _D = -4.1A		7.8	10.5	m0
Dialii-Source Oil-Resistance		V _{GS} = -2.5V, I _D = -3A		10.2	14	mΩ
Zero Gate Voltage Drain Current	loss	V _{DS} = -16V, V _{GS} = 0V			-1	μA
Gate-Source Leak Current	lgss	$V_{GS} = \pm 12V, V_{DS} = 0V$			±100	nA
Forward Voltage	V_{SD}	V _{GS} = 0V, I _S =-3A			-1.2	V
Gate Resistance	R _G	V _{DS} = 0V, f = 1MHz		2.5		Ω
Input Capacitance	C _{ISS}	V _{DS} = -8V, V _{GS} = 0V,		2053		
Output Capacitance	Coss	f = 1MHz		385		pF
Reverse Transfer Capacitance	C _{RSS}	I – IIVIOZ		338		
Total Gate Charge	Q _G	\\ - 45\\\\ - 0\\		38		
Gate to Source Charge	Q _{GS}	$V_{GS} = -4.5V, V_{DS} = -8V,$ $I_{D} = -15A$		6		nC
Gate to Drain Charge	Q _{GD}	- ID 15A		12		
Turn-on Delay Time	T _{D(ON)}			10		
Rise Time	Tr	$V_{GS} = -10V$, $V_{DS} = -8V$,		85		
Turn-off Delay Time	$T_{D(OFF)}$	$I_D = -13A, R_G = 27\Omega$		112		ns
Fall Time	T _f			110		
Diode Recovery Time	Trr	I _F =-20A, di/dt=-100A/us		23		ns
Diode Recovery Charge	Qrr	I _F =-20A, di/dt=-100A/us		14		nC



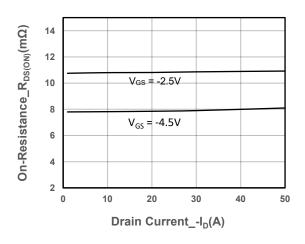
➤ Typical Performance Characteristics (T_A=25°C unless otherwise noted)

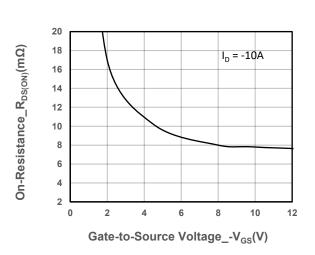




Output Characteristics

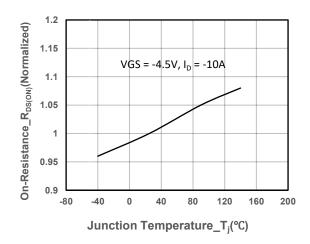


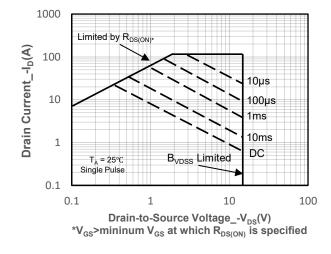




On-Resistance vs. Drain Current and Gate Voltag

On-Resistance vs. Gate-to-Source Voltage



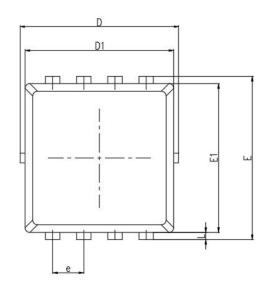


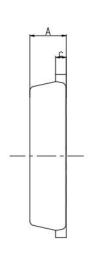
On-Resistance vs. Junction Temperature

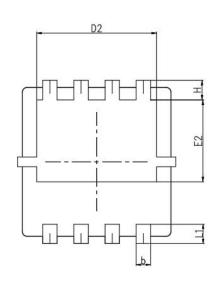
Safe Operating Area vs. Junction-to-Ambient

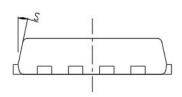


Package Information









Cumbal	MILL IMETER			
Symbol	Min	Nom	Max	
Α	0.65	0.75	0.9	
b	0.20	0.3	0.40	
С	0.1	1	0.22	
D	3.1	3.3	3.45	
D1	3	3.15	3.2	
D2	2.55	2.5	2.75	
E	3.15	3.3	3.45	
E1	2.9	3.05	3.2	
E2	1.55	1.75	1.95	
е	0.65BSC			
L	0.06	0.15	0.2	
L1	0.25	0.4	0.55	
Н	0.31	0.35	0.6	
S	10°	12°	14°	



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