SSC8045GS6

P-Channel Enhancement Mode MOSFET

➢ Features

V_{DS}	V_{GS}	$R_{DS(ON)}$ Typ.	I_D
-40V	±20V	80mΩ@-10V	-3A
		90mΩ@-4V5	

➢ Description

This device uses advanced trench technology to provide excellent RDSON and low gate charge . This device is suitable for use as a load switch,DC-DC conversion and power switch applications.

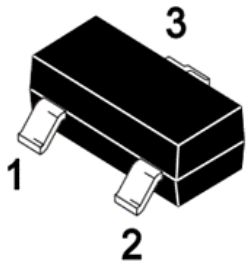
➢ Applications

- TFT panel power switch
- Portable DVD, DPF
- High side DCDC converter
- High side driver for brushless DC motor

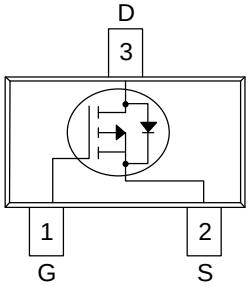
➢ Ordering Information

Device	Package	Shipping
SSC8045GS6	SOT-23	3000/Reel

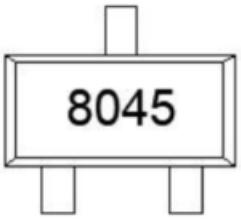
➢ Pin configuration



SOT-23



Pin Configuration (Top View)



Marking

➢ Absolute Maximum Ratings (T_A=25℃ unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain-to-Source Voltage	-40	V
V_{GSS}	Gate-to-Source Voltage	±20	V
I_D	Continuous Drain Current [a]	-3	A
I_{DM}	Pulsed Drain Current [b]	-12	A
P_D	Power Dissipation [c]	1.2	W
T_J	Operation junction temperature	-55~150	℃
T_{STG}	Storage temperature range	-55~150	℃

➢ Thermal Resistance Ratings (T_A=25℃ unless otherwise noted)

Symbol	Parameter	Typical	Maximum	Unit
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance [a]	110	150	℃/W

Note:

a. The value of $R_{\theta JA}$ is measured with the device mounted on 1 in^2 FR-4 board with 2oz.copper, in a still air environment with T_A=25℃.The value in any given application depends on the user is specific board design. The power dissipation is based on the t≤10s thermal resistance rating.

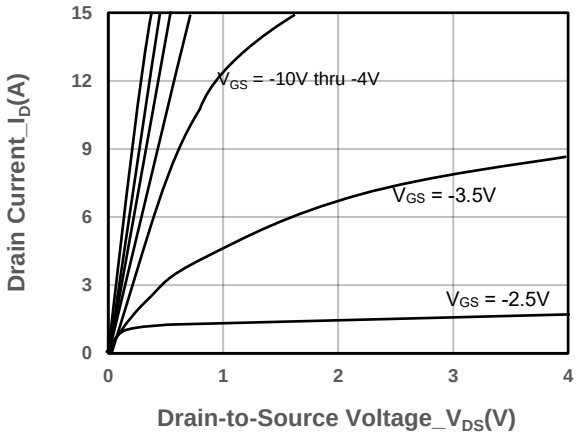
b. Repetitive rating, pulse width limited by junction temperature.

c. The power dissipation P_D is based on $T_{J(MAX)}$=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

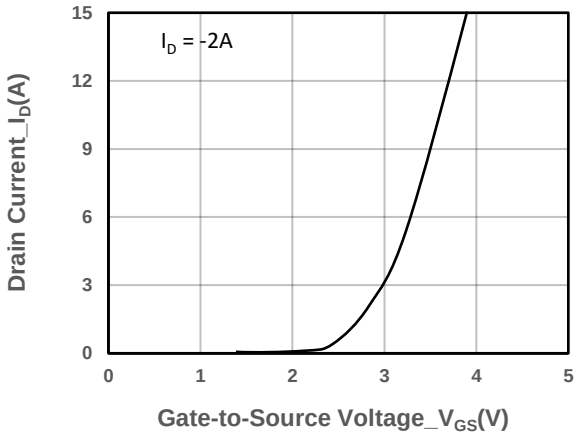
➢ Electrical Characteristics (T_A=25℃ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = -250uA	-40			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250uA	-1	-1.4	-2	V
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = -10V, I_D = -3A		80	105	mΩ
		V_{GS} = -4.5V, I_D = -2A		90	117	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -40V, V_{GS} = 0V			-1	uA
Gate-Source Leak Current	I_{GSS}	V_{GS} = ±20V, V_{DS} = 0V			±100	nA
Transconductance	G_{FS}	V_{DS} = -5V, I_D = -2A		8		s
Forward Voltage	V_{SD}	V_{GS} = 0V, I_S = -1A		-0.8	-1.3	V
Input Capacitance	C_{ISS}	V_{DS} = -20V, V_{GS} = 0V, f = 1MHz		587		pF
Output Capacitance	C_{OSS}			52.8		
Reverse Transfer Capacitance	C_{RSS}			45.9		
Turn-on Delay Time	$T_{D(ON)}$	V_{GS} = -10V, V_{DS} = -20V, I_D = -2A, R_G = 3Ω		6.5		ns
Rise Time	T_r			14		
Turn-off Delay Time	$T_{D(OFF)}$			35		
Fall Time	T_f			19		
Total Gate Charge	Q_G	V_{GS} = -10V, V_{DS} = -20V, I_D = -2A		7.8		nC
Gate to Source Charge	Q_{GS}			1.5		
Gate to Drain Charge	Q_{GD}			1.8		

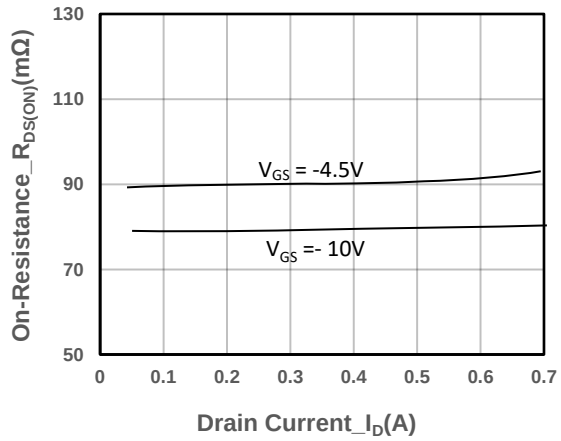
➢ Typical Performance Characteristics (T_A=25℃ unless otherwise noted)



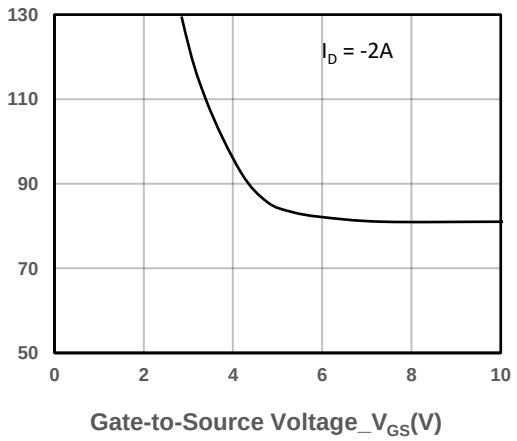
Output Characteristics



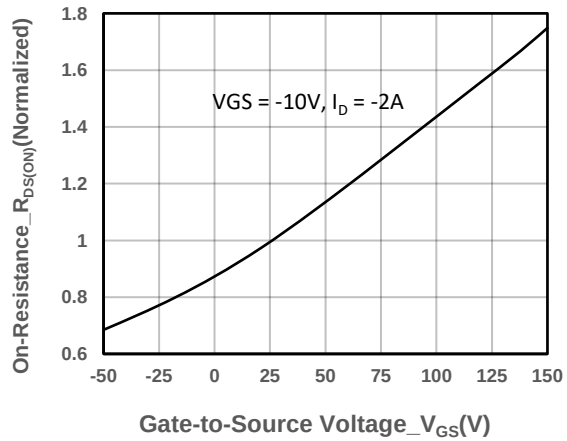
Transfer Characteristics



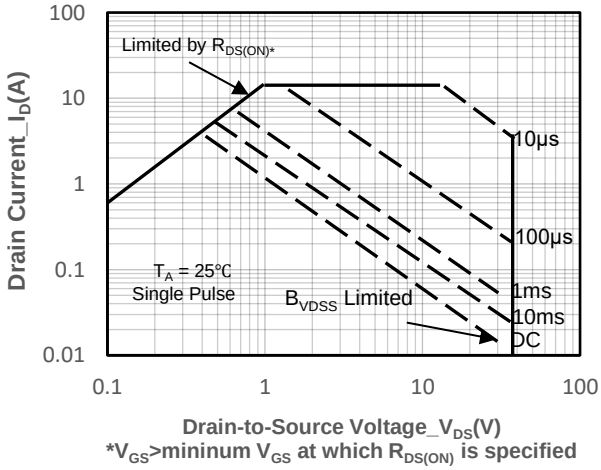
On-Resistance vs. Drain Current and Gate Voltag



On-Resistance vs. Gate-to-Source Voltage

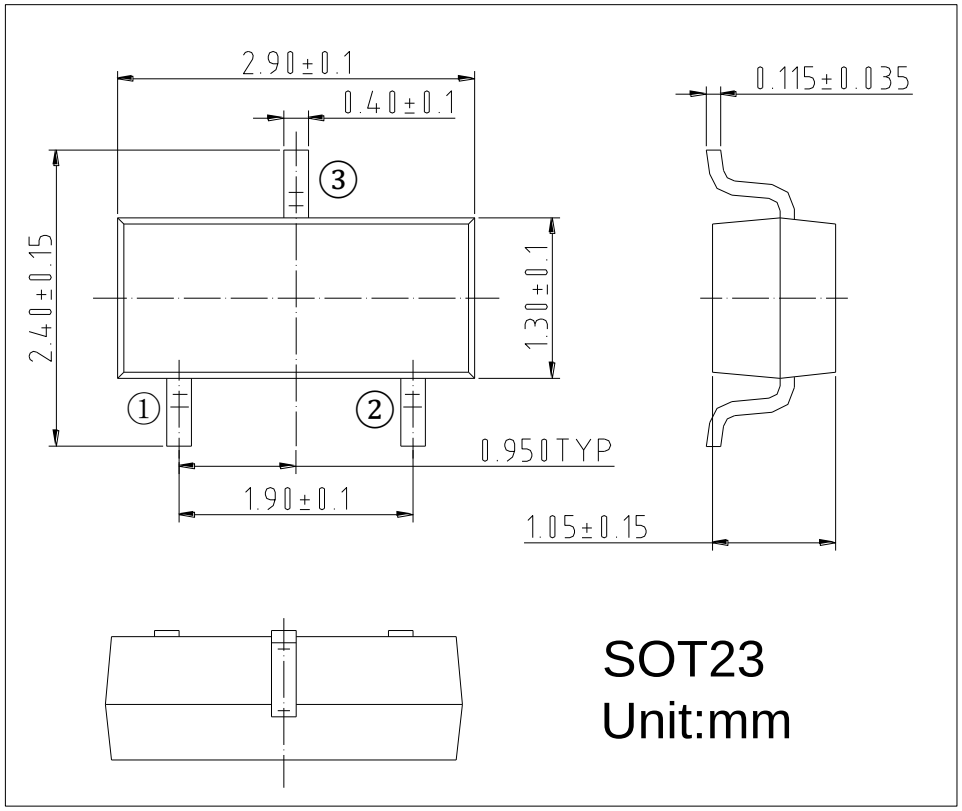


On-Resistance vs. Junction Temperature

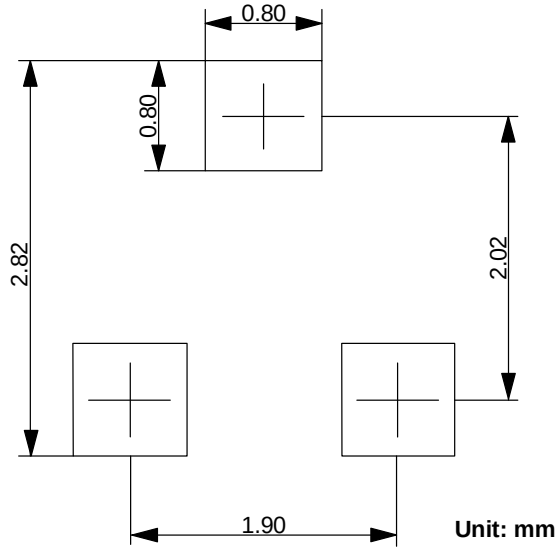


Safe Operating Area vs. Junction-to-Ambient

➢ Package Information



➢ Suggested Pad Layout



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